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CURRENT PULSE OVERLOAD TEST TO ASSURE THE RELIABILITY OF METALLIZED VIA HOLES IN ALUMINA SUBSTRATES

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ABSTRACT

The bilevel substrate designed for interconnecting integrated circuits utilizes a metallized alumina ceramic with laser drilled holes. The metallized through holes (via holes) establish electrical continuity between a metallized back plane, which serves as a very low inductance ground plane, and an upper metallized surface, which serves both power distribution and signal interconnection functions. Reliability of this circuit depends on the long term reliability of the via hole conductors.

Via holes are metallized by an evaporation process during which a 4000Å film of Au is deposited followed by an electroplating step to increase the Au film thickness to meet a resistance requirement. It is possible for a hole with nonuniform metallization to have an initial via hole resistance less than a required value, then upon aging this resistance will exceed the end of life requirement. A critical reliability problem arises in the limiting case of a hole which has a short annular plating void covered only by the evaporated metallization (4000Å, Au). This can be caused by entrapment of air

during electroplating. Failure to properly protect the hole with photoresist during etching can also lead to excessively thin gold at the rim of the hole.

To detect via holes in the bilevel substrate which have adequately low electrical resistance but short annular defects in the metallization each hole is subjected to a current pulse of sufficient magnitude to destroy, via I^2R heating, excessively thin metallization without harm to properly metallized via holes.

A quantitative heat analysis using several models relates the overload test parameters of current amplitude and pulse width required to open a conductor to the conductor's dimensions and the physical properties of the conductor and substrate. This analysis shows that the heat lost to the substrate is nearly equal to the heat generated with feasible overload parameters of current amplitude and pulse width. However, because the pulse width is short the total energy supplied is small while the peak power is large.

The minimum acceptable gold thickness in the via hole was determined to be 7000Å by extrapolating the results of a high temperature-short duration aging to a room temperature-long time (lifetime) performance.

An electrical overload test, which utilizes SCR's to gate the current pulses, was developed to assure a minimum via hole thickness. This test consists of two current pulses of 1 millisecond duration with a 1 millisecond interval between the pulses and a magnitude of 20 and 17 amperes respectively. If the metallized cross-sectional

area, defined by the product of the conductor thickness and the width of the circumferential metallization, is less than 5.6×10^{-6} cm^2 the area is destroyed. This cross-sectional area corresponds to a minimum thickness of 7000Å assuming the metallization covers the entire wall of the via hole. If the circumferential metallization covers less than 360^{o} of the via hole wall, the current pulse will destroy a metallization thickness greater than 7000Å.

Bilevel substrates with more than 7000Å of gold throughout the via hole that have been overload tested do pass an accelerated aging test which assures 40 year reliability.

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Via holes are metallized by an evaporation process during which a 4000Å film of Au is deposited followed by an electroplating step to increase the Au film thickness to meet a resistance requirement. It is possible for a hole with nonuniform metallization to have an initial via hole resistance less than a required value, then upon aging this resistance will exceed the end of life requirement. A critical reliability problem arises in the limiting case of a hole which has a short annular plating void covered only by the evaporated metallization (4000Å, Au). This can be caused by entrapment of air during electroplating. Failure to properly protect the hole with photoresist during etching can also lead to excessively thin gold at the rim of the hole.

To detect via holes in the bilevel substrate which have adequately low electrical resistance but short annular defects in the metallization each hole is subjected to a current pulse of sufficient

magnitude to destroy, via I^2R heating, excessively thin metallization without harm to properly metallized via holes.

A quantitative heat analysis using several models relates the overload test parameters of current amplitude and pulse width required to open a conductor to the conductor's dimensions and the physical properties of the conductor and substrate. This analysis shows that the heat lost to the substrate is nearly equal to the heat generated with feasible overload parameters of current amplitude and pulse width. However, because the pulse width is short the total energy supplied is small while the peak power is large.

The minimum acceptable gold thickness in the via hole was determined to be 7000Å by extrapolating the results of a high temperature-short duration aging to a room temperature-long time (lifetime) performance.

An electrical overload test, which utilizes SCR's to gate the current pulses, was developed to assure a minimum via hole thickness. This test consists of two current pulses of 1 millisecond duration with a 1 millisecond interval between the pulses and a magnitude of 20 and 17 amperes respectively. If the metallized cross-sectional area, defined by the product of the conductor thickness and the width of the circumferential metallization, is less than 5.6×10^{-6} cm^2 the area is destroyed. This cross-sectional area corresponds to a minimum thickness of 7000Å assuming the metallization covers the entire wall of the via hole. If the circumferential metallization covers less

than 360° of the via hole wall, the current pulse will destroy a metallization thickness greater than 7000Å.

Bilevel substrates with more than 7000Å of gold throughout the via hole that have been overload tested do pass an accelerated aging test which assures 40 year reliability.

I. INTRODUCTION

The complexities of integrated circuits has increased the demands on the interconnection of the IC's. The use of a bilevel substrate can alleviate many of the design difficulties encountered in meeting the stringent electrical requirements of interconnections. For example, a bilevel substrate offers (1) a controlled characteristic impedance of signal lines, (2) a reduced inductance of the ground circuit, (3) a reduced resistive drop in the ground circuit, (4) a reduced signal line cross talk, and 5) increased packing density of I.C. elements.

For these reasons, a bilevel substrate was developed by the Bell Telephone Laboratories. The bilevel substrate is basically an alumina ceramic circuit board. The alumina ceramic is the dielectric between the metallization on both sides of the substrate. There are laser drilled holes in the substrate which are also metallized. These metallized through holes (via holes) establish electrical continuity between a metallized back plane which serves as a very low inductance ground plane and an upper metallized surface which serves both power distribution and signal interconnect functions. The reliability of the via hole conductors is a very important aspect of the overall circuit reliability.

The via hole resistance is not of itself a sufficient criterion to assure long term reliability of the via hole conductor. It is possible for a hole with nonuniform metallization to have an initial via hole resistance less than the required value; then upon

aging this resistance will exceed the end of life requirement. A critical reliability problem, as shown in Figure 1, arises in two cases of nonuniform metallization: 1) entrapment of air during electroplating can cause a short annular plating void covered only by the evaporated metallization, as shown in Figure 1a; and 2) failure to properly protect the hole with photoresist during an etching procedure can lead to excessively thin gold at the rim of the hole, as shown in Figure 1b.

To guarantee that holes in a manufactured bilevel substrate have adequate minimum thickness of gold to satisfy long-term reliability requirements an electrical overload current test was developed for the bilevel substrate. This test can detect via holes in the bilevel substrate which have adequately low electrical resistance but short annular defects in the metallization by subjecting each hole to a current pulse of sufficient magnitude to destroy, via I^2R heating, excessively thin metallization.

This paper is a discussion of an electrical test to ensure the long term reliability of metallized via holes in the bilevel substrate. The significant parts to be covered are 1) a quantitative heat analysis of the via hole overload test, 2) the experimental determination of the overload test conditions, and 3) the circuit design of the overload test.

II. QUANTITATIVE HEAT ANALYSIS

The purpose of the heat analysis of the via hole overload test is to relate the effects of the overload test parameters, which

are the pulse width and amplitude, the via hole conductor dimensions and the physical properties of the conductor and substrate, to the opening of the via hole conductor.

A. Model and Theoretical Considerations

The model used for this analysis is shown in Figure 2. The following assumptions are used to simplify the analysis:

1) The opening of the gold conductor occurs upon melting. Therefore the heat required to open the conductor consists of the heat necessary to raise the gold to the melting temperature plus the heat of fusion. There are too many variables, mainly a changing area due to necking down of the gold, to extend the analysis through to evaporation.

2) The physical properties remain constant during heating. The properties as listed in Figure 2 are the average values over the temperature range of 1040°C, which is the change in temperature between the ambient temperature and the melting point of gold.

3) The metallization system, although it consists of Ti-Pd-Au, will be assumed to be only Au. Typical thicknesses are 1000Å Ti, 1000Å Pd, and 5,000 to 50,000Å Au.

4) Heat loss from the gold conductor is by conduction only.

5) No temperature gradient exist through the gold thickness.

6) No temperature drop exist at the metal-ceramic interface.

There are five cases to be considered. For the no loss case, the heat generated by the electric current is consumed by the

metal in increasing its temperature (storing heat). In the four lossy cases, the heat loss will be the difference between the heat generated by the electric current and the heat stored by the metal.

1. No Heat Loss Case

$$Q_{generated} = Q_{stored}$$

$$I^2Rt = c_1 m\Delta T + mL_{F1}$$

$$I^2 \frac{\rho_1 \ell}{\pi d\tau} t = \delta_1 \pi d\ell\tau \ (c_1\Delta T + L_{F1})$$

Solving for I

$$I = \left(\frac{\pi^2 d^2 \tau^2 \delta_1 \ (c_1\Delta T + L_{F1})}{t \rho_1}\right)^{1/2} \qquad (1)$$

2. Heat Loss Cases

Before starting the analysis the assumption of considering the alumina substrate rather than the gold conductive back plane as the heat sink must be justified. The heat flow or heat rate by conduction is

$$\frac{dQ}{dt} = - kA \frac{dT}{dn}$$

The temperature gradient $(\frac{dT}{dn})$ for both the substrate and the back plane is the same. Therefore the product of the thermal conductivity (k) and the area (A) must be compared for both the substrate and the back plane.

Substrate $A_2 = \pi d\ell = 5.08 \times 10^{-3}$ cm^2

$k_2 = 0.094$ watt/cm^{o}K

$A_2k_2 = 4.77 \times 10^{-4}$ watt-cm/^{o}K

Back plane $A_1 = \pi d\tau = 8 \times 10^{-2}\ \tau$ cm

$k_1 = 2.8$ watt/cm^{o}K

$\tau = 1\mu m$, $A_1k_1 = 2.24 \times 10^{-5}$ watt-cm/^{o}K

$\tau = 5\mu m$, $A_1k_1 = 1.12 \times 10^{-4}$ watt-cm/^{o}K

With the back plane gold thickness varying between 1 μm to 5 μm the heat flow to the substrate is 4 to 20 times greater than to the back plane. Therefore the substrate will be considered as the heat sink, where the temperature gradient and heat flow are in the radical direction.

The exact solution of a transient heat conduction in two different materials including internal heat generation in cylindrical co-ordinates has not been found in the literature. Therefore solutions of different classical heat transfer models will be evaluated for quantification of the overload test parameters of pulse width and amplitude, the via hole conductor dimensions, and the physical properties of the conductor and substrate, to the opening of the via hole conductor.

2.1 One dimensional heat conduction in unsteady state of a sudden temperature change at the surface of an infinitely thick ceramic plate.

Total heat lost to the substrate[1]

$$Q = 2\, k_2\, \pi d \ell \Delta T \sqrt{\frac{t}{\pi \alpha_2}}$$

$$Q_{loss} = Q_{generated} - Q_{stored}$$

$$2\, k_2 \pi d \ell \Delta T \sqrt{\frac{t}{\pi \alpha_2}} = I^2 \frac{\rho_1\, \ell\, t}{\pi d \tau} - \delta_1 \pi d \ell \tau\, (c_1\, \Delta T + L_{F1})$$

Solving for I

$$I = \left(\frac{\pi^2\, d^2\, \tau^2\, \delta_1\, (c_1\, \Delta T + L_{F1})}{t\, \rho_1} + \frac{2\pi^2\, d^2\, k_2\, \Delta T\, \tau}{\rho_1 \sqrt{\pi \alpha_2}\, \sqrt{t}} \right)^{1/2} \qquad (2)$$

2.2 One dimensional heat conduction in unsteady state with constant heat flux at the surface of an infinitely thick ceramic plate.

Temperature at the surface of the substrate is given by[2]

$$T = \frac{2H}{k_2} \left(\frac{\alpha_2 t}{\pi} \right)^{1/2} \qquad (3)$$

Heat flux (H) is defined as the rate at which heat is transferred across a surface per unit area per unit time. The heat flux lost to the substrate is then the difference between the heat generated and the heat stored per unit area per unit time.

$$\frac{Q_{loss}}{\pi d \ell t} = \frac{Q_{generated}}{\pi d \ell t} - \frac{Q_{stored}}{\pi d \ell t}$$

$$H = \frac{I^2 \rho_1}{\pi^2 d^2 \tau} - \delta_1 \frac{\tau}{t} (c_1 \Delta T + L_{F1}) \qquad (4)$$

Equation 3 is derived for a constant heat flux. The determined heat flux, equation 4, is a function of t and ΔT. In order to use equations 3 and 4 to solve for I, it will be assumed that the generated heat flux is much greater than the stored heat flux, this is the actual case as is proven later. Then H in equation 4 will represent a constant heat flux.

Equating equations 3 and 4 and solving for I

$$I = \left(\frac{\pi^2 d^2 \tau^2 \delta_1 (c_1 \Delta T + L_{F1})}{t \rho_1} + \frac{\pi^3 d^2 k_2 \Delta T \tau}{2 \rho_1 \sqrt{\pi \alpha_2} \sqrt{t}} \right)^{1/2} \qquad (5)$$

2.3 Heat conduction in a cylindrical hole with constant heat flux at the substrate surface. The surface temperature is giving by[3]

$$T = \frac{2H}{\pi k_2} \int_0^\infty (1 - e^{-\alpha_2 \mu^2 t}) \frac{J_o(\mu a) Y_1(\mu a) - Y_o(\mu a) J_1(\mu a)}{\mu^2 [J_1^2(\mu a) + Y_1^2(\mu a)]} d\mu \qquad (6)$$

where H is defined as before in equation 4, J_o and J_1 are Bessel functions of the first kind, Y_o and Y_1 are Bessel functions of the

second kind, a is the radius of the hole and μ is an integrating variable

Solving for I from equations 4 and 6

$$I = \left(\frac{\pi^2 d^2 \tau^2 \delta_1 (c_1 \Delta T + L_{F1})}{t \rho_1} + \frac{\pi^3 d^2 k_2 \Delta T \cdot \tau}{2 \rho_1 \int_0^\infty (1-e^{-\alpha_2 \mu^2 t}) \frac{J_o(\mu a) Y_1(\mu a) - Y_o(\mu a) J_1(\mu a)}{\mu^2 [J_1^2(\mu a) + Y_1^2(\mu a)]} d\mu}\right)^{1/2} \quad (7)$$

2.4 One dimensional heating of a thin metal film on a substrate by a constant heat flux. The temperature at the metal-ceramic interface is given by[4]

$$T = \frac{2H}{k_1} (\alpha_1 t)^{1/2} \left(\frac{1}{\sqrt{\pi}} + \sum_{n=1}^{\infty} 2(-m)^n \text{ ierfc } \frac{n \tau}{(\alpha_1 t)^{1/2}}\right) \quad (8)$$

where $$m = \frac{\frac{k_2}{\sqrt{\alpha_2}} - \frac{k_1}{\sqrt{\alpha_1}}}{\frac{k_2}{\sqrt{\alpha_2}} + \frac{k_1}{\sqrt{\alpha_1}}}$$

and where the heat flux (H) is defined as before in equation 4.

Solving for I from equations 4 and 8

$$I = \left(\frac{\pi^2 d^2 \tau^2 \delta_1 (c_1 \Delta T + L_{F1})}{t \rho_1} + \frac{\pi^2 d^2 k_1 \Delta T \tau}{2\rho_1 \sqrt{\alpha_1 t} \left[\frac{1}{\sqrt{\pi}} + \sum_{n=1}^{\infty} 2(-m)^n \text{ ierfc } \frac{n \tau}{(\alpha_1 t)^{1/2}}\right]}\right)^{1/2} \quad (9)$$

B. Discussion

Five equations have been derived for the five classical heat transfer models using the stated assumptions. Since the material of the substrate (Al_2O_3) and of the conductor (Au) and the dimension of the hole (assuming uniform metallization in the hole) have been defined there are three variables remaining in the equations. These are the two overload test parameters which are the pulse width (t) and amplitude (I), and the thickness (τ) of the conductor which is to be destroyed by this test. The effect of these three variables can be observed when the appropriate properties and dimension, Figure 2, are used in equations 1, 2, 5, 7 and 9.

Equation 1 No Loss Case 1

$$I = \left(3.38 \times 10^{-2} \frac{\tau^2}{t} \frac{sec}{\mu m^2}\right)^{1/2} \text{ amp}$$

Equation 2 Lossy Case 2.1 - Constant Surface Temperature - One Dimensional

$$I = \left(3.38 \times 10^{-2} \frac{\tau^2}{t} \frac{sec}{\mu m^2} + 63.6 \frac{\tau}{\sqrt{t}} \frac{sec}{\mu m}^{1/2}\right)^{1/2} \text{ amp}$$

Equation 5 Lossy Case 2.2 - Constant Heat Flux - One Dimensional

$$I = \left(3.38 \times 10^{-2} \frac{\tau^2}{t} \frac{sec}{\mu m^2} + 50. \frac{\tau}{\sqrt{t}} \frac{sec}{\mu m}^{1/2}\right)^{1/2} \text{ amp}$$

Equation 7 Lossy Case 2.3 - Constant Heat Flux - Cylindrical Hole.

$$I=\left(3.38\times10^{-2}\,\frac{\tau^2}{t}\,\frac{\text{sec}}{\mu m^2}+\frac{1.24\times10^{5}\,\tau}{\int_0^{\infty}(1-e^{-\alpha_2\mu^2 t})\,\frac{J_o(\mu a)Y_1(\mu a)-Y_o(\mu a)J_1(\mu a)}{\mu^2[J_1^2(\mu a)+Y_1^2(\mu a)]}\,d\mu}\right)^{1/2}\text{amp}$$

Equation 9 Loss Case 2.4 - Constant Heat Flux - Thin Film - One Dimensional

$$I=\left(3.38\times10^{-2}\,\frac{\tau^2}{t}\,\frac{\text{sec}}{\mu m^2}+\frac{1.185\times10^{2}\,\tau\;\;\text{Sec}^{1/2}\,\mu m^{-1}}{\sqrt{t}\,\left(\frac{1}{\pi}+\sum_{n=1}^{\infty}2(-m)^n\,\text{ierfc}\,\frac{\tau}{(\alpha_1 t)^{1/2}}\right)}\right)^{1/2}\text{amp.}$$

Notice that the first term in Equations 2, 5, 7 and 9 is the no-loss term for the energy to open the conductor; i.e., the results of equation 1, while the second term in all the equations is the lossy term. Another way of looking at the results of the lossy cases is to think of the total current supplying two components. The first component is that required to melt (open) the conductor while the second component is that which is lost in supplying heat to the substrate.

The three variables remaining in the equations are two overload test parameters of t and I and the thickness τ. Thus to open a specific thickness (τ) either t or I can be chosen and the other determined. The initial criterion used was to fix the pulse width at a value equal to the time which produces a 10% heat loss from the conductor to the substrate. One of the four lossy equations must be used to determine the pulse width. For ease of calculation,

the choice can be reduced to equations 2 and 5. Since equations 2 and 5 are nearly equal and case 2.2 more nearly represents the actual situation in the via hole as compared to case 2.1, equation 5 will be used to determine the pulse width. Results of equation 5 for a gold thickness (τ) of 1 μm, and several pulse widths are presented in Table 1 below. The no loss term is the current component required to open the 1 μm thick conductor while the lossy term is the current component which causes heating in the substrate.

TABLE 1

	No Loss Term	Lossy Term	I amp.
$t = 10^{-10}$ sec	3.38×10^{8}	$5. \times 10^{6}$	1.85×10^{4}
10^{-9} sec	3.38×10^{7}	1.58×10^{6}	5.95×10^{3}
10^{-8} sec	3.38×10^{6}	$5. \times 10^{5}$	1.97×10^{3}
10^{-6} sec	3.38×10^{4}	$5. \times 10^{4}$	3.9×10^{2}
10^{-3} sec	3.38×10^{1}	1.58×10^{3}	4.02×10^{1}

Results of these calculations show that to avoid any loss of heat to the substrate the overload pulse should be an impulse of current, but this is impossible.

The result of these calculations show that if only 10 percent of the heat required to open the hole is lost to the substrate, the theoretical pulse width required is then in the range of 10^{-9} to 10^{-8} seconds, and the corresponding current amplitude is in the order 2×10^{3} to 6×10^{3} amperes. Both the pulse width and current amplitude are physically unattainable. These calculations indicate that

the amount of heat lost to the substrate will be larger than that required to open the via hole (without loss) with reasonable overload parameters of current amplitude and pulse width. The pulse width chosen was 10^{-3} seconds because it was easily achieved.

A comparison of the four lossy cases will be made to determine the magnitude of the required current to open a 1 μm gold thickness with the pulse width fixed at 1 millisecond, see Table 2, below. In all four cases with $t = 10^{-3}$ sec, the lossy term is dominant. The required current for cases 2.1, 2.2 and 2.4 was calculated using equations 2, 5 and 9, respectively. The required current for case 2.3 was determined numerically with the use of Figure 1 of Lardner and Pohle's paper.[5]

TABLE 2

Case		Required Current (I)
2.1	One dimensional, constant surface temperature	45.2 amps
2.2	One dimensional, constant heat flux	40.2 amps
2.3	Cylindrical, constant heat flux	44.8 amps
2.4	One dimensional, constant heat flux	40.1 amps

The results of Table 2 indicate the greatest heat loss is for Case 2.1. This is expected since the heat loss is proportional to the temperature gradient and the temperature gradient is greater with a constant surface temperature than with a constant heat flux. Also note the cylindrical geometry with constant heat flux, 2.3, has a

larger Heat loss than the one dimensional case, 2.2. This can be accounted for as an increase in area with an increase in penetration depth of the cylindrical geometry. Now comparing the two one dimensional cases with constant heat flux, 2.2 and 2.4, the required current is nearly equal although the solutions are derived from two different approaches. In case 2.2 the heat loss to the substrate is a function of the thermal properties of the substrate whereas in case 2.4, the loss is a function of the thermal properties of the thin gold film.

The effects of the hole conductor dimensions on the current required to cause an opening of the conductor can now be discussed. Since the lossy term is dominant, with $t = 10^{-3}$ seconds, this term in equations 2, 5, 7 and 9 will be discussed. The required current is directly proportional to the diameter of the conductor and to the square root of the thickness of the conductor. The length of the conductor does not appear in either of the terms in any of the equations.

The analysis of the four lossy cases yield similar results with the pulse width, $t = 10^{-3}$ seconds. Therefore limits can be placed on the required current to open the via hole conductor using the no loss case, equation 1, for the lower limit and the one dimensional constant heat flux lossy case, equation 5 for the maximum limit. A plot of these calculations is shown in Figure 3.

III. EXPERIMENTAL DETERMINATION OF THE OVERLOAD TEST CONDITIONS

A result of the quantitative heat analysis, with the pulse width set to 10^{-3} seconds, has placed limits on the current required to open the via hole conductor, as shown in Figure 3. The experimental determination of the current amplitude of the overload test consisted of 1) generating an empirical curve of the current required to open a via hole metallization versus the gold thickness in the via hole, and 2) determining the minimum reliable thickness of metallization in the via hole.

The procedure for the empirical determination of the current amplitude of the overload test as a function of via hole gold thickness consisted of sample preparation, overload testing and determining the gold thickness.

Bilevel substrates were prepared with different gold thicknesses over normal thicknesses of titanium and palladium. The gold thickness was adjusted by varying both the amount of gold deposited during evaporation and by varying the length of time in electroplating. These samples were then subjected to the overload test. The pulse width of the overload test was set at 1 millisecond, as was discussed previously, while the current amplitude was adjusted until approximately 80% of the holes tested on a given substrate were destroyed. The reason for destroying a large number of holes was based on the thesis that a thickness distribution exists, and this distribution would be skewed toward the lower thicknesses. Therefore by destroying 80% of the holes the remaining holes would have a uniform

thickness which would make the determination of the gold thickness easier. After being overload tested the metallized substrates were cross sectioned for examination by scanning electron microscopy.

Scanning electron micrographs of two holes which were destroyed by the overload test are shown in Figure 4. The thickness of the metallization of the hole shown in Figure 4a is less than the critical thickness for the entire length of the hole. The metallization in the hole shown in Figure 4b, however, had a thickness less than the critical thickness for only about 2/3 of its length. Micrographs of a hole in the same substrate from which the above two holes were taken are shown at two different magnifications in Figure 5. This hole passed the overload test. A gold thickness of 8000Å was measured from the 10K magnification micrograph.

The results of the above procedure were used to obtain the overload current amplitude versus gold thickness curve in Figure 6. The empirical curve is between the minimum and maximum limits determined from equations 1 and 5. This empirical curve brackets the range of thicknesses that were measured from via holes which had passed the overload test. The spread between these two curves is the result of two factors. First, the thicknesses measured from micrographs of via holes not destroyed by the overload test must be equal to or greater than the thicknesses destroyed by the test. Second, the opening of the via hole conductor is a function not only of conductor thickness but also the degree of coverage of the hole by the evaporated gold metallization; i.e. the amount of metallization around

the perimeter of the via hole. Both of these factors are a result of the nonuniformity of evaporated metallization in the via hole. The nonuniformity in evaporated metallization could also account for the discrepancy between the theoretical lossy curve and the upper empirical curve. This can be supported since it is known that as the metallization thickness is increased by plating, the metallization within the hole becomes very uniform. This is shown in Figure 6 where the empirical curve approaches the lossy curve as the metal thickness is increased. The upper empirical curve then represents the minimum uniform thickness, with 360^{o} coverage, which will be destroyed by the overload test. If the circumferential metallization covers less than 360^{o} of the via hole wall, then the current pulse will destroy a greater thickness of metallization.

The total energy applied to a substrate to open a 1 μm thick uniform via hole using the results of Figure 6 is 5.2×10^{-2} joules. The total energy is small while the peak power is large at 52 watts.

The current-thickness curve of Figure 6, is a function of the pulse width, t, as indicated previously. The time necessary to open a via hole, assuming the current amplitude is constant, is dependent on the area of metallization normal to the length of the via hole. The current pulse through the via hole was monitored to observe when the metallization was opened. The waveforms of the current pulse through four via holes are shown in Figure 7. The widest pulse did not open the via hole but the other three holes were opened

as indicated by an early turn off time and subsequent arcing. The shortest pulse width corresponds to a via hole with the smallest area of metallization.

In the development of the overload test, a problem emerged over the shape of the overload current pulse. The overload current pulse had an overshoot at the trailing edge which was inherent to the overload circuitry. The overshoot amplitude was approximately 40% greater than the test current amplitude and the pulse width of this overshoot was about 20 μ seconds. The consequence of this overshoot was to cause many via holes to open on this sudden surge of energy. The overshoot was reduced with a circuit modification, as will be discussed later, so the overload test could be more easily specified without considering the effects of the overshoot.

A phenomenon of the overload test was observed wherein it is possible for a via hole to open in subsequent tests of a repetitive pulse testing scheme. This phenomenon occurs because there exists a thickness (actually an area), slightly greater than the one that is destroyed, which is heated and melts, but before this area can open the current ceases. This area is deformed due to necking upon melting resulting in a smaller area upon cooling. This smaller area on a subsequent test will be destroyed. This phenomenon results in the overload test being a potentially destructive test. The procedure of eliminating this reduced area is to test the via hole with a second current pulse which would destroy this reduced area but would

not deform any other areas. The amplitude of the second pulse was determined to be between 80 and 90% of the first pulse. The time between pulses should be greater than 1 millisecond to avoid any heat accumulation in the conductor. Figure 8 shows an example where this two current pulse program caused five holes to open in the first pulse and one hole to open on the second pulse. A few hundred via holes which had passed this two pulse overload test were subjected to repetitive overload testing of 10 pulses at the second pulse amplitude without having one via hole fail.

After having determined the overload test procedures of two current pulses, reducing the current overshoot and having determined a current-thickness curve, the minimum acceptable thickness of metallization in the via hole must be determined so that the overload test current amplitude could be chosen.

The actual experimental determination of the minimum reliable thickness is complicated by two factors. They are: (1) difficulty in coating a via-hole uniformly with less than 7,000Å ~ 10,000Å of metallization. (2) Difficulty in accurately measuring an actual film thickness of less than 7000Å ~ 10,000Å in the hole. Therefore, about 7000Å of Au was the minimum thickness for which the reliability of a via-hole conductor could be experimentally determined.

The minimum reliable thickness was determined by aging 3 substrates with a respective gold thickness of 7000, 8000 and 12,000Å (the gold was in each case deposited on top of 1000Å Ti and

1000Å Pd). The gold thickness in the via-holes was determined from scanning electron micrographs (10,000X magnification) of the cross sections of the gold film as was shown in Figure 5b.

The gold film thickness in via-holes can be estimated from the via-hole resistance assuming a uniform film coverage in the hole. The estimated thicknesses are listed in Table 3 below together with the film thicknesses on the substrate surface estimated from the sheet resistance measurement and the film thickness measured on the SEM. The agreement between the calculated values of gold film thickness and the measured values is good. Table 3 also shows that the gold tends to be somewhat thinner in the via-hole than on the substrate surface. This is reasonable since shadowing during evaporation leads to a thinner gold film inside the hole.

TABLE 3

Gold Thickness on the Substrate Surface and in the Via-Hole

Sample No.	Gold Thickness On the Surface*	In the Via-Hole**	In the Via-Hole***
6-18-70-A6	8,200Å	7,000Å	7,000Å
6-19-70-A8	10,000Å	8,000Å	9,000Å
7-15-70-B4	12,000Å	12,000Å	11,000Å

* Determined from sheet resistance.
** Determined from via-hole resistance.
*** Direct reading from SEM photomicrographs.

The via hole resistance was measured with a four-point probe test set. The number of holes tested in a substrate is indicated in Table 4.

These samples were aged in air at 350°C for 124 hours or 137 hours. The via-hole resistances before and after the aging treatments are tabulated in Table 4.

TABLE 4

Via-Hole Resistances Before and After Aging at 350°C in Air

Time	Via-Hole Resistance (Ω) Min.	Ave.	Max.	Increase in Ave. Via-Hole Resistance
Sample No. 6-18-70-A6 (48 Holes)				
0 Hrs.	0.027	0.035	0.051	49%
137 Hrs.	0.030	0.052	0.085	
Sample No. 6-19-70-A8 (43 Holes)				
0 Hrs.	0.021	0.027	0.043	26%
124 Hrs.	0.021	0.034	0.056	
Sample No. 7-15-70-B4 (50 Holes)				
0 Hrs.	0.011	0.015	0.022	53%
137 Hrs.	0.011	0.023	0.043	

In all samples, the average via-hole resistances increased after aging. The increase ranged from 26% for sample 6-19-70-A8 to 53% for sample 7-15-70-B4.

If a single thermally activated mechanism for conductor film deterioration is assumed, and if a reasonable value of activa-

tion energy for this mechanism (say 0.5 eV) is assumed, then one can extrapolate the result of a high temperature-short time test to a room temperature-long (life) time performance.[6] In this time-temperature equivalent method,[7,8] 40 years at 60°C is equivalent to 100 hours at 350°C assuming an activation energy of 0.5 eV. Thus within the limits of the above assumptions, the via-hole resistance increase during the lifetime of the circuit should be less than that observed in the extrapolation from the accelerated aging experiment. The results from the three test samples indicated that even for a via-hole Au film thickness as low as 7000Å, the resistance increase is less than a factor of 2 (0.052Ω/0.035Ω = 1.5). Therefore, if a minimum thickness of 7000Å is specified, the end-of-life (40 year) resistance will be less than twice the initial resistance. However, this does mean that the via-hole resistance required on the initially manufactured bilevel substrate must be less than 0.67 of the end of life resistance value to insure reliability of the via hole.

The 7000Å Au film thickness was accepted as the minimum Au thickness in the via hole because of the following three factors. They are: 1) Of the samples life tested, none of the holes opened; i.e. the via hole resistance did not exceed 1 KΩ. 2) The increase in via hole resistance of all the samples due to aging was approximately the same. 3) Film thicknesses less than 7000Å in the via hole were very nonuniform and the reliability of these films was unattainable.

Now that the minimum acceptable thickness of metallization in the via hole has been determined to be 7000Å, the current amplitude

values of the overload test can be determined with the use of Figure 6. The first current pulse amplitude should be 20 amperes while the second current pulse amplitude should be 85% of the first pulse or 17 amperes.

The final consideration was to determine the effects of the overload test on long term reliability of the via hole conductor. To insure that the current pulse overload test did not degrade via holes with more than the minimum required thickness of metal, several bi-level substrates that had been overload tested were subjected to accelerated aging at 350°C for 140 hours. The increased resistance of metal films in the via holes in these substrates was no more than that observed for the untested substrates with comparable gold thickness in the via hole, indicating that the overload test had no adverse effect on the via hole conductor.

IV. DESIGN OF THE VIA HOLE OVERLOAD TEST SET

The approach taken was to use a silicon controlled rectifier to gate the high amplitude, short duration current pulse for the destruction of metallization in via holes with less than the minimum acceptable thickness.

A. Basic SCR DC Switch

The silicon controlled rectifier (SCR) is an undirectional device (current flows from anode to cathode only) and has three terminals - anode, cathode and control gate. Assuming zero voltage applied to the control gate the SCR is in the high impedance or "off" state. The SCR is switched to its low impedance or "on" state by

applying a positive voltage to the control gate with sufficient current to forward bias the junction. Once in saturation the anode current is limited only by the external circuit. Once the gate has been used to trigger the SCR into conduction the gate loses control, and the only method of turning conduction off is to reduce the anode current below the holding current level. This can be achieved by either opening the anode circuit or reversing the anode to cathode voltage.

The basic SCR DC switch[9] is shown in Figure 9. Resistors R_1 and R_2 are chosen for the desired currents. The capacitor C is used to reverse bias the SCR's, one at a time, to turn them off. Assume SCR_1 has been turned on and SCR_2 is in the "off" state. The anode of SCR_1 is at a low voltage while the anode of SCR_2 is at the source voltage since SCR_2 is off and there is no voltage drop across R_2. Thus the source voltage is across the capacitor C having a polarity of minus (-) at SCR_1 and plus (+) at SCR_2. This d-c condition of SCR_1 conducting and SCR_2 nonconducting will exist until SCR_2 is turned on. Now assume that the voltage applied to the gate of SCR_1 is zero while a positive pulse is applied to the gate of SCR_2 which turns SCR_2 on. At this point both SCR's are conducting, but as soon as SCR_2 is turned on the voltage across the capacitor C, which is equal to the source voltage, reverse biases SCR_1 thus turning SCR_1 off. Now SCR_2 is on and SCR_1 is off and the capacitor charges to the value of the source voltage with the polarity of plus (+) at the anode of SCR_1 and minus (-) at the anode of SCR_2. This condition

will exist until SCR_1 is turned on; then the voltage across the capacitor would reverse bias SCR_2, turning it off. This discussion explains why the SCR D-C switch utilizes two SCR's and a capacitor to produce a current of a fixed duration through both of the resistors.

To control the operation of the SCR D-C switch both SCR's cannot conduct at the same time except for the transition time while each SCR changes state. There are two conditions that must be observed so that both SCR's don't remain in the "on" state, for once they both remain "on" the only method for resetting the off-on operation is to turn the supply voltage off. The two conditions to be observed are: 1) both gate signals cannot be positive at the same time, and 2) the time constants R_1C and R_2C must be properly limited in value. For the first condition if both gates are turned on when the reversing voltage of the capacitor forward biases the SCR, the SCR will remain on. Now both SCR's are conducting and control of the circuit is lost. To avoid this situation the controlling pulses to the gates of the SCR's should not overlap. One should be high while the other is low. For the second condition, the minimum time constant is determined by the "turn off time", t_{off}, specified for the SCR. The turn off time (see Figure 10) is defined as the minimum time interval between zero current (the instant the SCR is reversed biased) and the time of reapplication of a forward biasing anode-cathode voltage under specified conditions which will cause the device to remain in the off state after having been in the on-state. This can be explained further with the use of the sketch in Figure

10. At t = o SCR1 is reversed biased to -V after having been in the on state. The voltage across SCR1 changes exponential to +V. The minimum time between t = o and the time when the voltage across SCR1 reaches zero volts while still keeping SCR1 in the off state is the turn off time. Thus, if the SCR is in the "on" state and the reversing voltage across the SCR reaches zero volts a time interval greater than the turn off time, the SCR will be in the off state, but if the reversing voltage across the SCR reaches zero volts in a time interval less than the turn off time, the SCR will remain in the on state. To calculate the minimum time constant, τ, involves calculating the time constant necessary for the voltage to reach zero volts in the time equal to t_{off} as the capacitor charges from -V to +V, where V equals the supply voltage, Figure 10.

The minimum time constant is 1.45 times t_{off}. The maximum time constant is determined by the period of time the SCR is on. During this "on" time the capacitor must reverse polarity, a change in voltage of twice the source voltage. If τ_{max} equal 1/3 period the SCR is on, the capacitor voltage will charge to 90% of the source voltage. If the voltage to which the capacitor charges is too low (say τ > 1/2 period), then the voltage to reverse bias the SCR reaches zero voltage in a time less than t_{off} and the SCR will remain in the "on" state. In summary, the product of R and C should be greater than 1.45 t_{off} but less than 1/3 the period the SCR is on.

B. Bilevel Via Hole Overload Prototype

The SCR D-C switch was selected to provide the high current pulse for the bilevel overload test because both the amplitude and pulse width can be controlled independently. The prototype test set was designed with a common plate for electrical contact to the back plane of the metallized bilevel substrate and a hand probe to make electrical contact to the metallized pads on the front side of the bilevel substrate. The via hole to be tested was placed in series with SCR_1, Figure 11, which is normally in the "off" state while SCR_2 is in the "on" state. The test cycle is initiated and SCR_1 conducts for 1 millisecond then is switched back to the "off" state. The amplitude of the overload current can be controlled by adjusting either the source voltage or the resistance, R_1, in series with the via hole. The duration of the overload current pulse is controlled by the control circuit used to drive the gates of the SCR's and is adjusted by varying the time between turning SCR_1 "on" and turning SCR_2 "on". The control pulses are obtained from a monopulser. The meter, M, in series with the via hole indicates whether or not the hole was tested. R_3 was added so that the capacitor is charged to the source voltage to avoid arcing at the via hole when the probe first makes contact to the metallized pad.

Design considerations will be discussed in general terms. Figure 11 contains the actual values and calculations used in the prototype overload test set.

1. Power Supply for the SCR D-C switch should provide sufficient voltage and current. The required voltage of the supply is determined by the required current through the via hole and the value of resistance R_1. The minimum current of the power supply can be determined from R_2 and the source voltage. The minimum current limit can only be used if the power supply has a slow transient response time to large current surges. For example, the prototype circuit takes 1 ampere for nearly 100% of the duty cycle while it takes 20 amperes for 1 millisecond. Therefore the transient response time of the power supply should be greater than 10 milliseconds. If the supply has a fast transient response time the required current should be equal to the current through the via hole.

2. SCR Rating.

   (a) Minimum Forward Breakover Voltage should exceed the value of the source voltage.

   (b) Forward current rating should exceed the current through SCR_2. It need not exceed the current through the via hole since the duty cycle of SCR_1 is very small.

   (c) Turn off time, t_{off}, must be known for determining the value of the capacitor, C. The turn off time should be small, say less than 15 μ seconds.

3. Control circuit for turning the SCR's "on". A knowledge of the gate triggering specifications of the SCR is necessary so the proper voltage and current can be supplied by the control circuits.

4. Determination of R_1, R_2, C.

   R_1 determines the amplitude of the current pulse, while C is determined from the value of t_{off} and R_1. The minimum value of C is used so the maximum value of R_2 can be used to obtain the minimum current through SCR_2. R_2 is determined from the value of C and the time period for which SCR_1 is on.

5. The value of R_3 was determined from the R_3C time constant so that C is fully charged in the period of time between testing two via holes.

C. Discussion

The current pulse for the via hole from the SCR D-C switch is shown in Figure 12a. The overshoot at the trailing edge of the pulse is due to the charging of the capacitor, C. This overshoot is undesirable from an application standpoint and was reduced by a circuit modification. The modified SCR D-C switch produced a current pulse with reduced overshoot as shown in Figure 12b. The modification of the SCR D-C switch, as shown in Figure 13, was accomplished by providing a lower resistance path for charging the capacitor during the turnoff time on SCR_1. The third SCR (#3) is turned on at the same time SCR_2 is turned on. SCR_3 is turned off when the voltage across R_1 decreases to zero volts, i.e. when the SCR_1 is off. A diode, D_1, is necessary between the gates of SCR_2 and SCR_3 in order to limit leakage current through the via hole under test.

As was determined, the overload test for the via hole of the bilevel substrate should consist of two current pulses. The

amplitude of the second pulse should be less than that of the first. There are two methods of obtaining a second current pulse of lower amplitude than the first: 1) the power supply can be programmed to decrease its voltage, and 2) the resistance in series with the via hole could be increased. The choice of methods depends on the sequence of testing the via holes. Since the minimum time between pulses was sought and remote programming of the power supply required approximately 100 milliseconds to stabilize the new voltage level, the second method was chosen. To accomplish this two SCR D-C switches share the same via hole to be tested, as shown in Figure 14. SCR's 1 and 3 produce the first current pulse of 20 amperes while SCR's 2 and 4 produce the second current pulse of 17 amperes. The second pulse amplitude is adjusted by the 10Ω pot. The pulse widths, 1 millisecond each, of these two pulses is controlled by the width of the gating pulses applied to SCR's 1 and 3 and SCR's 2 and 4 respectively. The time delay between these two pulses is controlled by the time between the gating pulses to SCR1 and SCR2.

Figure 15 shows a block diagram of the complete overload test set. It consists of a control unit, the SCR drivers, and the SCR D-C switch; respectively shown in Figures 16, 17 and 14. The SCR drivers were necessary because the control unit used integrated circuits and couldn't supply the current required to turn on the SCR's. The drivers also provided buffering for the control circuitry. The control unit provides the timing necessary to determine the width of both of the overload current pulses and the delay between them.

Mono 1 and Mono 3 control the width of the first and second overload current pulse respectively, while Mono 2 determines the delay between them. The input of Mono 1 is a delay circuit which initiates the test cycle. The test cycle is initiated by the switch S and this delay circuit provides both a delay and a clean noise free pulse to prohibit any switch noise from causing a false start.

V. SUMMARY

The long term reliability of a metallized via hole in the bilevel substrate which passes the electrical overload test can be assured. The two current pulse overload test is a nondestructive test for holes which pass the test. Neither the reliability of the metallization nor of the substrate is affected by the test if the cross-sectional area of metallization exceeds the minimum area corresponding to the test conditions.

A quantitative heat analysis using several models has related the overload test parameters of current amplitude and pulse width required to open a conductor to the conductor's dimensions and the physical properties of the conductor and substrate.

The heat analysis has shown that the heat loss to the substrate is nearly equal to the heat generated with feasible overload parameters of current amplitude and pulse width. However, because the pulse width is short the total energy is small while the peak power is large. The required current to open the conductor is independent of conductor length, directly proportional to the diameter of the conductor and to the square root of the conductor thickness.

The heat analysis of four lossy cases yield similar results. Therefore limits were placed on the required current amplitude to open the conductor using the no loss case for the lower limit and the one dimensional constant heat flux lossy case for the maximum limit. One could use these general equations for other via hole dimensions, metallization and substrate materials to determine a current pulse overload test for any metallized via hole.

The experimental data of the required current to open a specific thickness are between the theoretical upper and lower limits determined from the heat analysis. The spread in these data is a result of the nonuniform evaporated metallization around the perimeter of the via hole. At the 20 ampere current amplitude the overload test did open (destroyed) metallized thicknesses of 7000Å and 11,000Å. The 7000Å thickness corresponds to 360° of metallization, while the 11,000Å thickness corresponds to 290° of metallization within the via hole. Therefore this overload test guarantees a minimum cross-sectional area of metallization and thus a minimum gold thickness everywhere within the via hole.

The minimum acceptable gold thickness in the via hole was determined to be 7000Å. The corresponding overload test conditions are two current pulses of 1 millisecond in duration and a 1 millisecond interval between them. The amplitudes of the first and second pulses are 20 and 17 amperes, respectively.

The SCR D-C switch was chosen to perform the current switching function of the overload test. The basic operation of the SCR D-C

switch was explained. The prototype overload test set with design considerations was discussed. The basic SCR D-C switch was modified to reduce the overshoot and was used to produce the two current pulse overload test.

The overload test is presently being used in the laboratory as a diagnostic test and in manufacturing as an attribute test.

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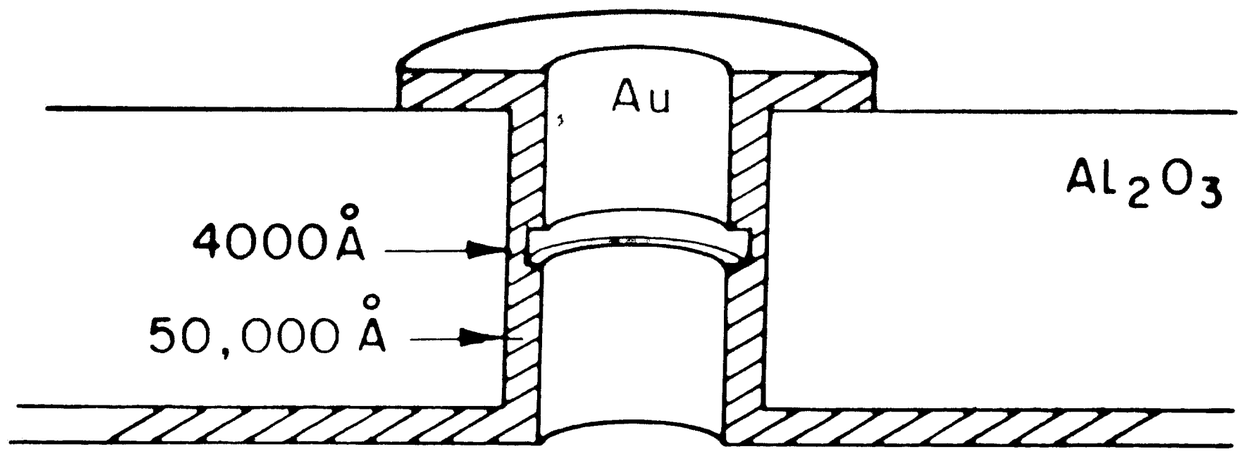
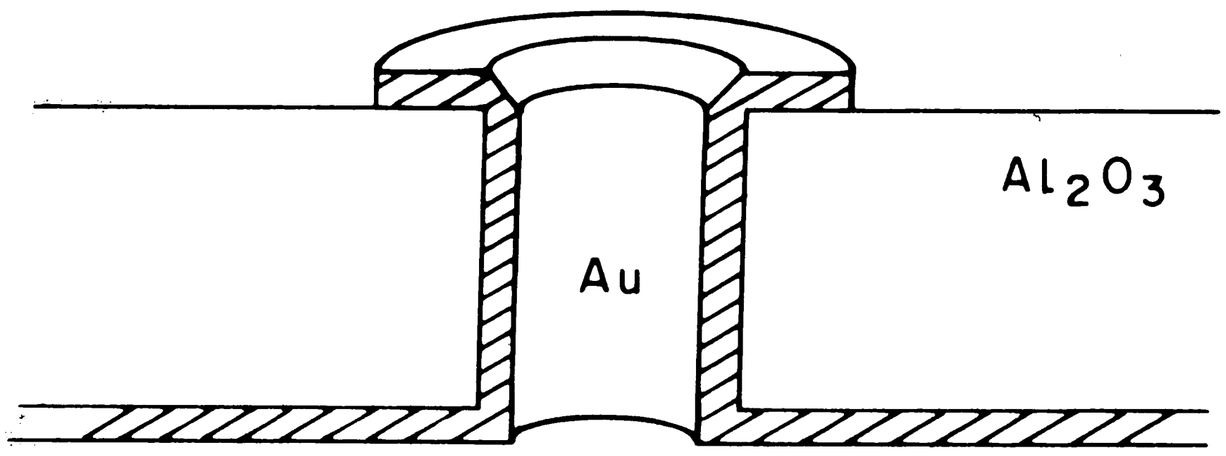


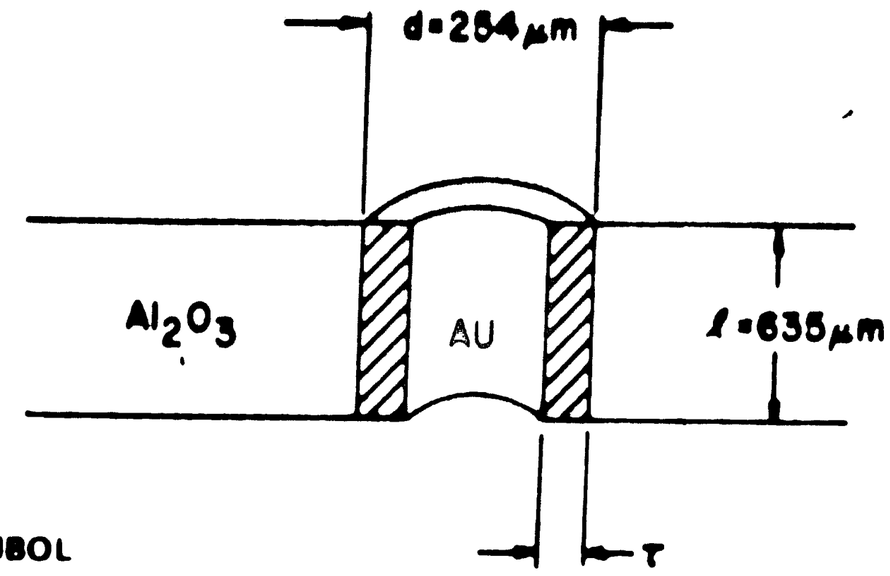
(a) SHORT ANNULAR PLATING VOID



(b) THIN METALLIZATION AT RIM OF HOLE

TWO CASES OF NONUNIFORM METALLIZATION

FIGURE 1



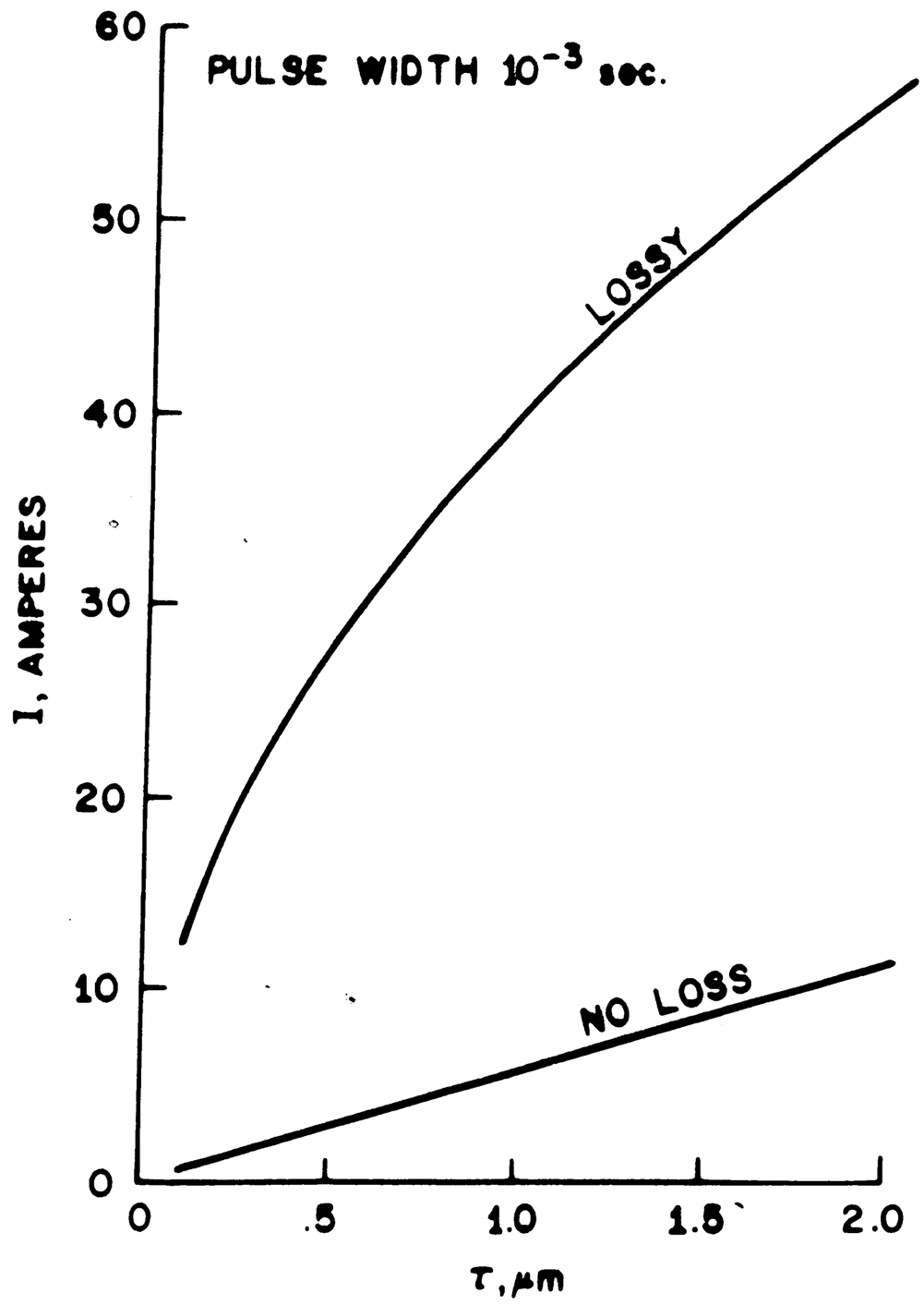
SYMBOL		*REFERENCE
Q.	HEAT	
H.	HEAT FLUX	
ΔT.	CHANGE IN TEMPERATURE, 1040°K	
I.	CURRENT	
t.	PULSE WIDTH	
ℓ.	LENGTH OF VIA HOLE CONDUCTOR	
d.	DIAMETER OF VIA HOLE CONDUCTOR	
T.	THICKNESS OF VIA HOLE CONDUCTOR	
δ_1.	Au. DENSITY 19 3 gm cm3	1
ρ_1.	Au. RESISTIVITY 7 8 x 10^{-6} Ω cm	1
c_1.	Au. SPECFIC HEAT 0 142 JOULES gm°K	1
k_1.	Au. THERMAL CONDUCTIVITY 2 8 watt cm°K	1
α_1.	Au. DIFFUSIVITY 1 01 cm^2 sec	
L_{F1}.	Au. LATENT HEAT OF FUSION 67 2 JOULES gm	2
k_2.	Al_2O_3. THERMAL CONDUCTIVITY 0 094 watt/cm°K	1
α_2.	Al_2O_3. DIFFUSIVITY 0.02 cm^2/sec	

*REFERENCE

1 THERMOPHYSICAL PROPERTIES OF HIGH TEMPERATURE SOLID MATERIALS, VOLUMES 1 AND 4 I

2 METALS HANDBOOK, 1948 EDITION
MODEL AND PROPERTIES FOR QUANTITATIVE HEAT ANALYSIS

FIGURE 2



OVERLOAD TEST
THEORETICAL CURRENT THICKNESS CURVE

FIGURE 3

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B71-5838-AL

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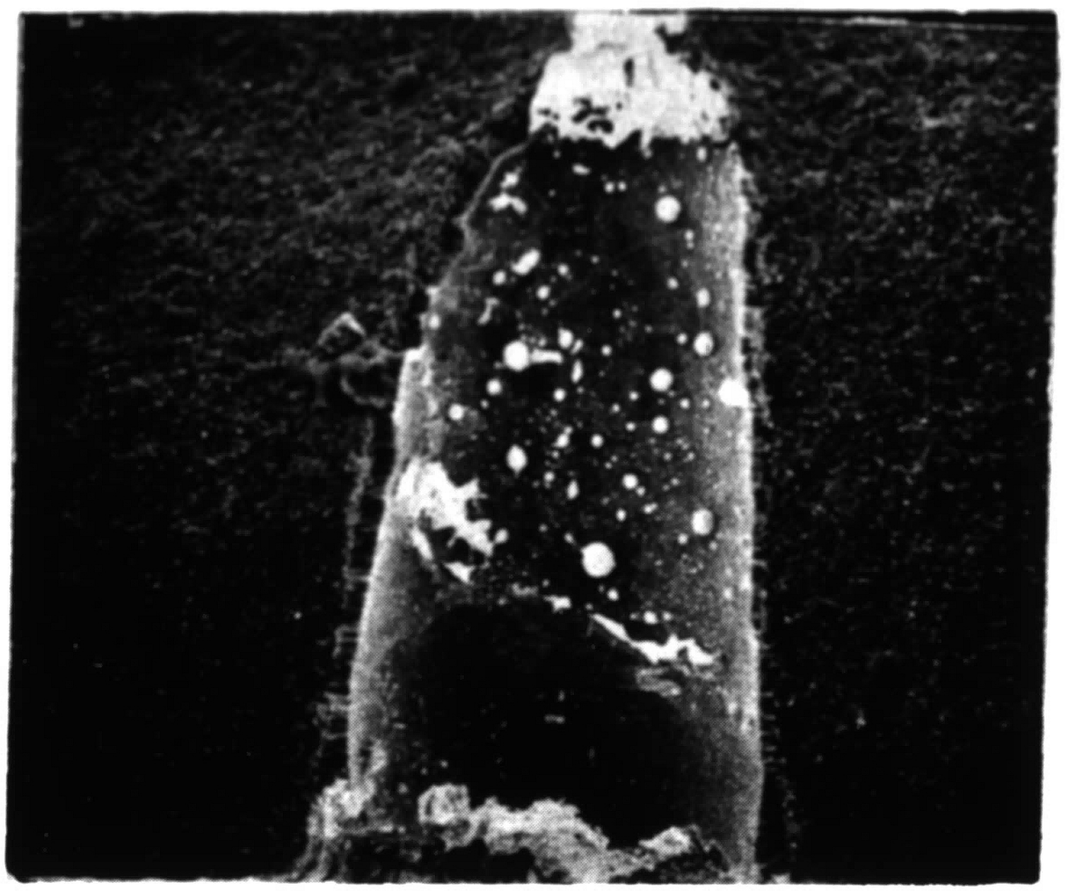
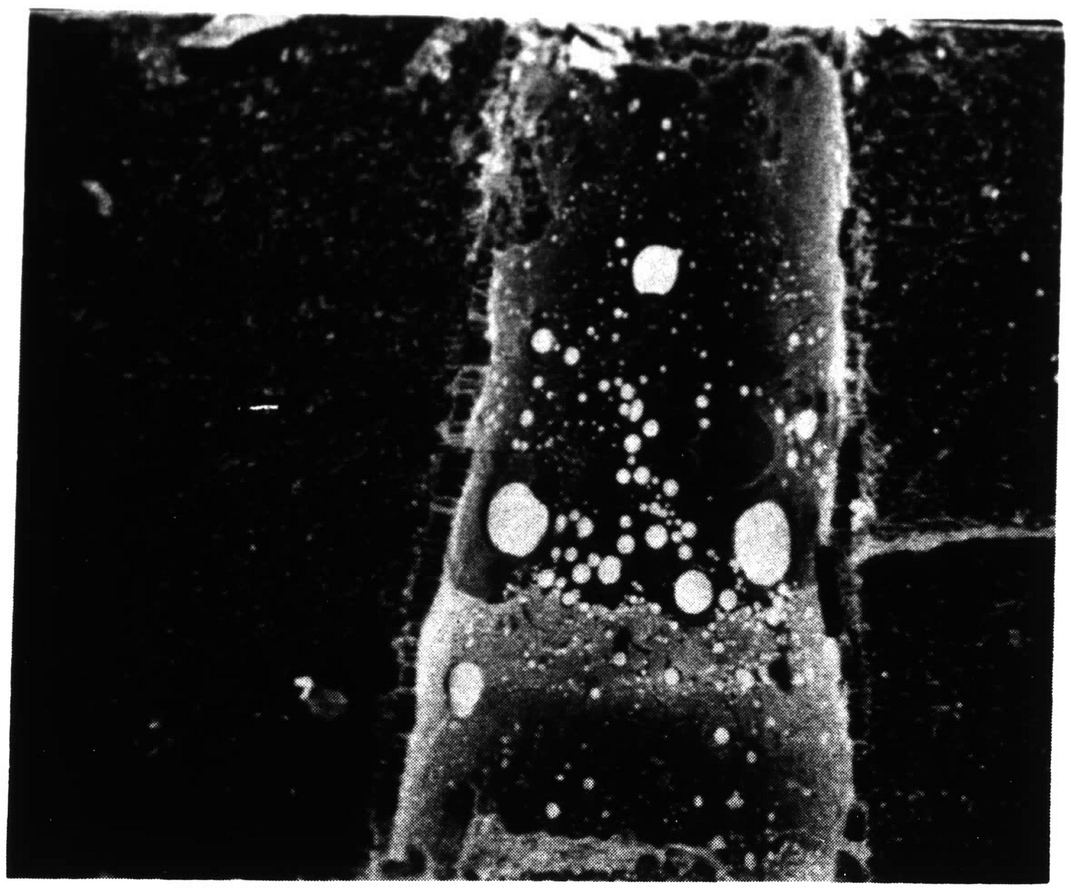
CASE NO.
39514-2



4(a) 100X



4(b) 100X

SCANNING ELECTRON MICROGRAPHS
TWO BURNED OUT HOLES

FIGURE 4

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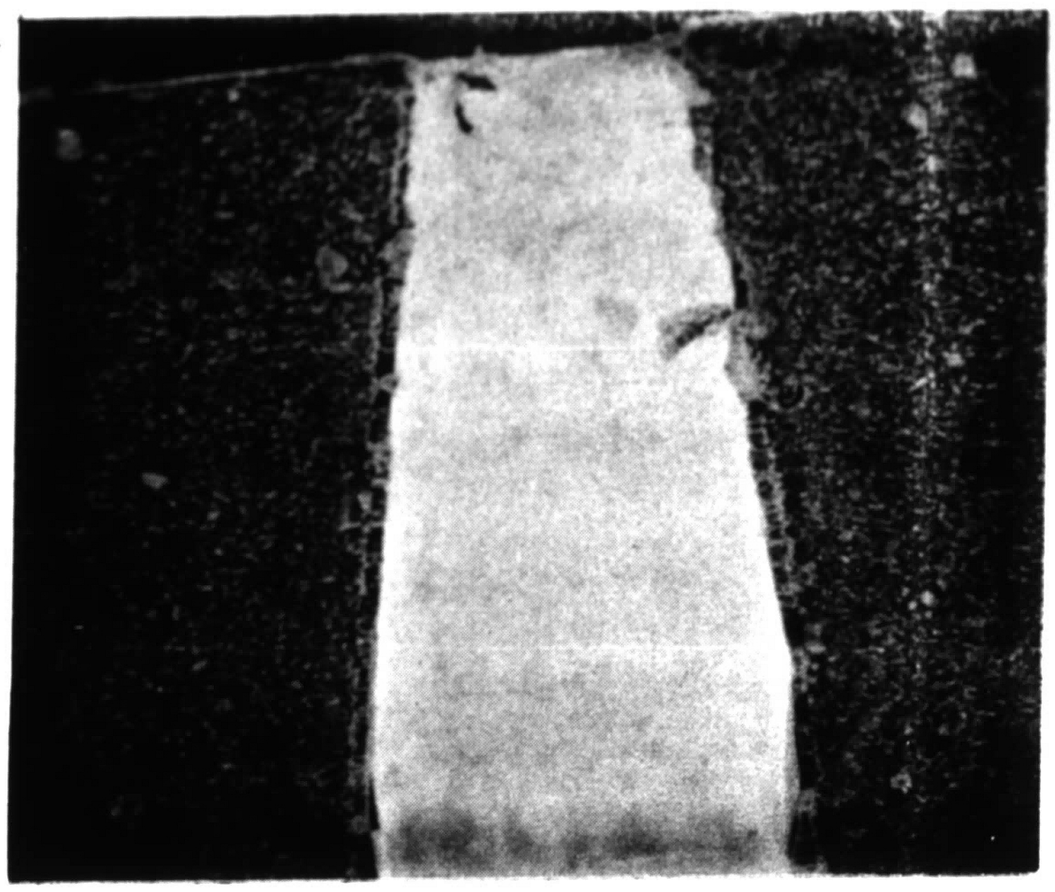
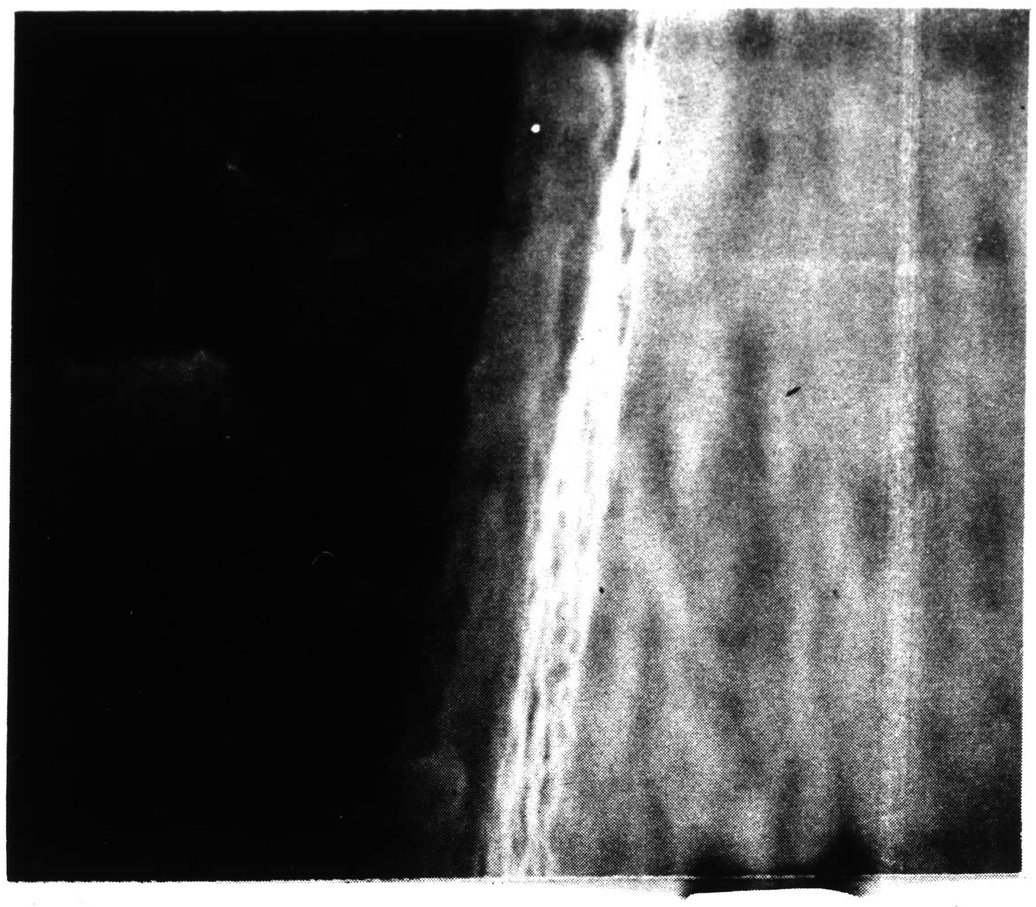


5 (a) 100X



5(b) 10KX

SCANNING ELECTRON MICROGRAPHS OF A HOLE THAT PASSED THE OVERLOAD TEST

FIGURE 5

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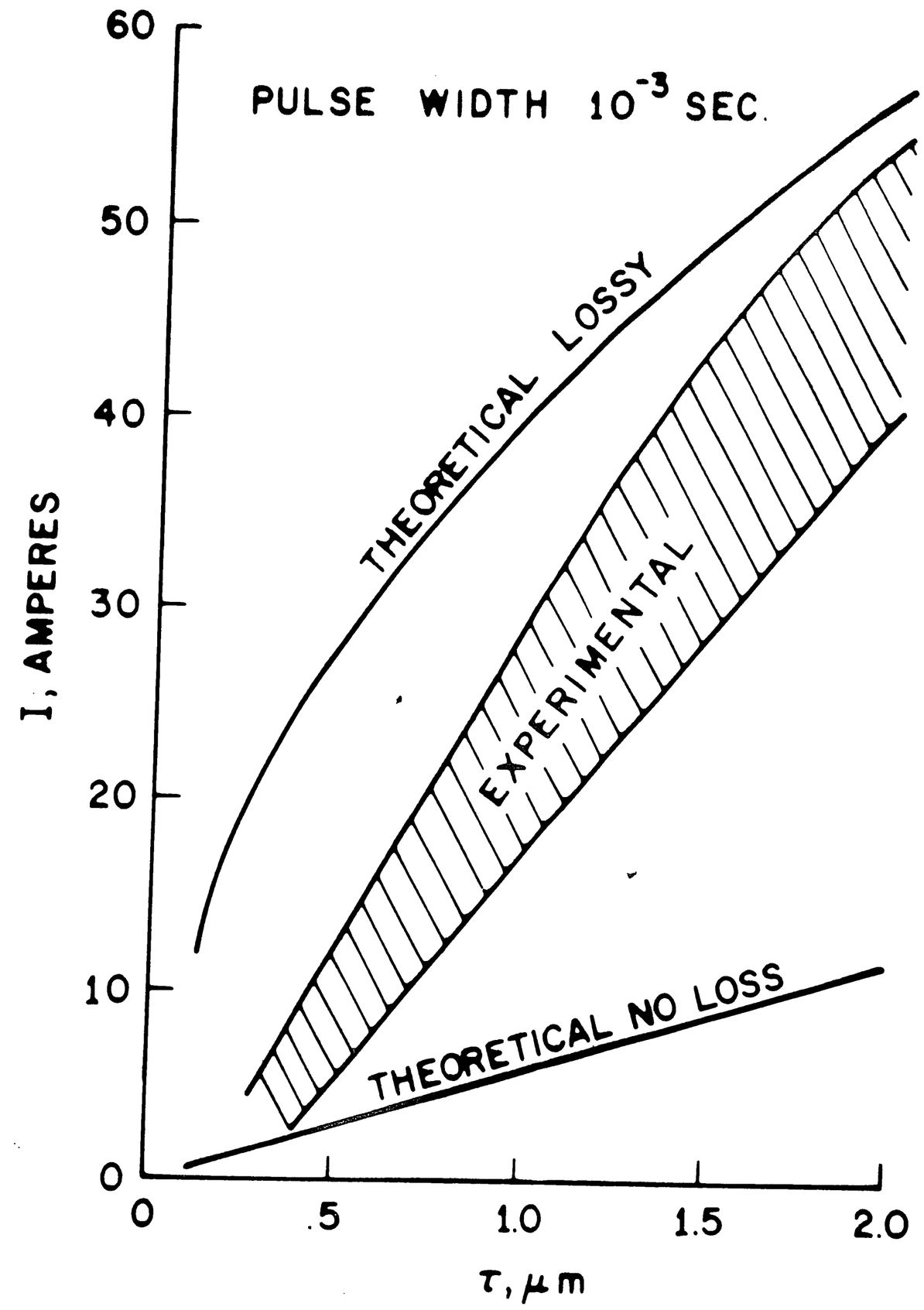

OVERLOAD TEST
CURRENT THICKNESS CURVE

FIGURE 6

PHOTO NO.
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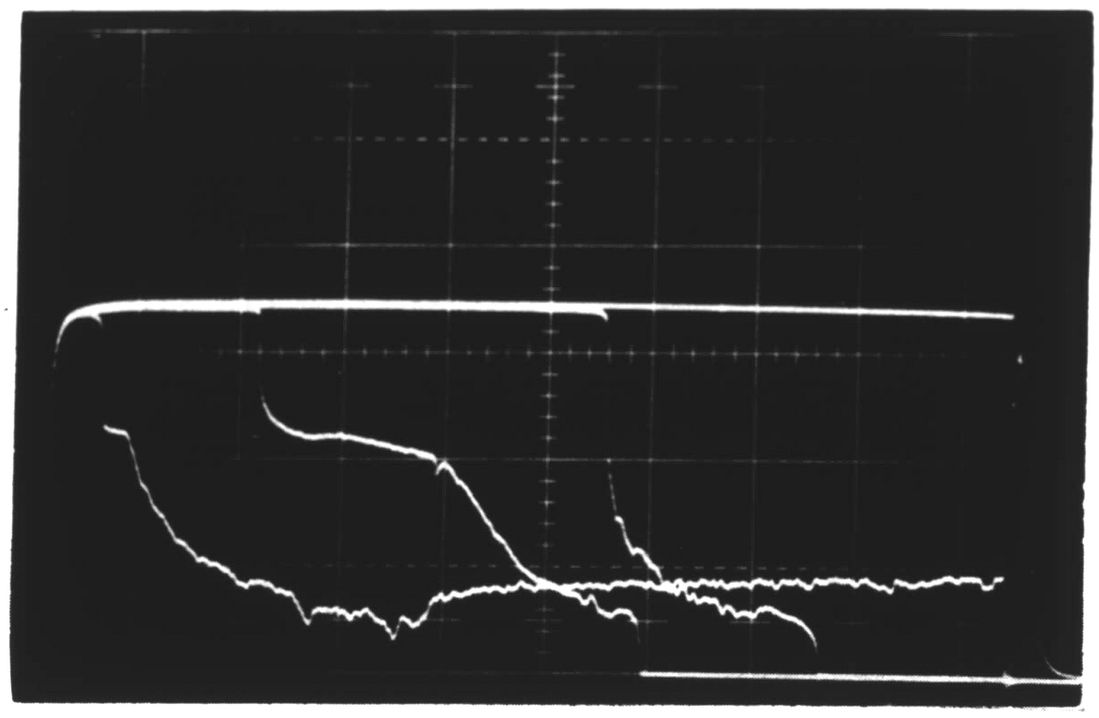
SCALE:

VERT. 5A/cm

HOR. 0.1 m sec. / cm



OVERLOAD TEST WAVEFORMS
OF FOUR HOLES

FIGURE 7

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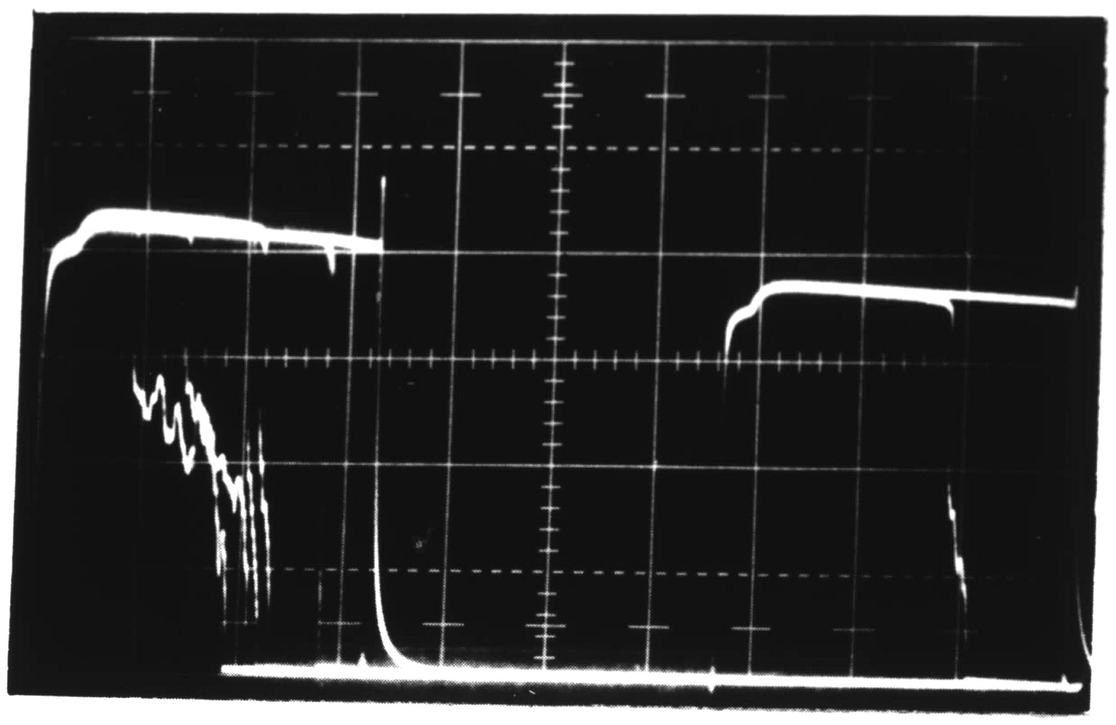
39514-2

PHOTO NO.
B72-1244-AL

SCALE:

VERT. 5A/cm
HOR. UNCAL



TWO PULSE OVERLOAD TEST WAVEFORMS
OF SEVEN HOLES

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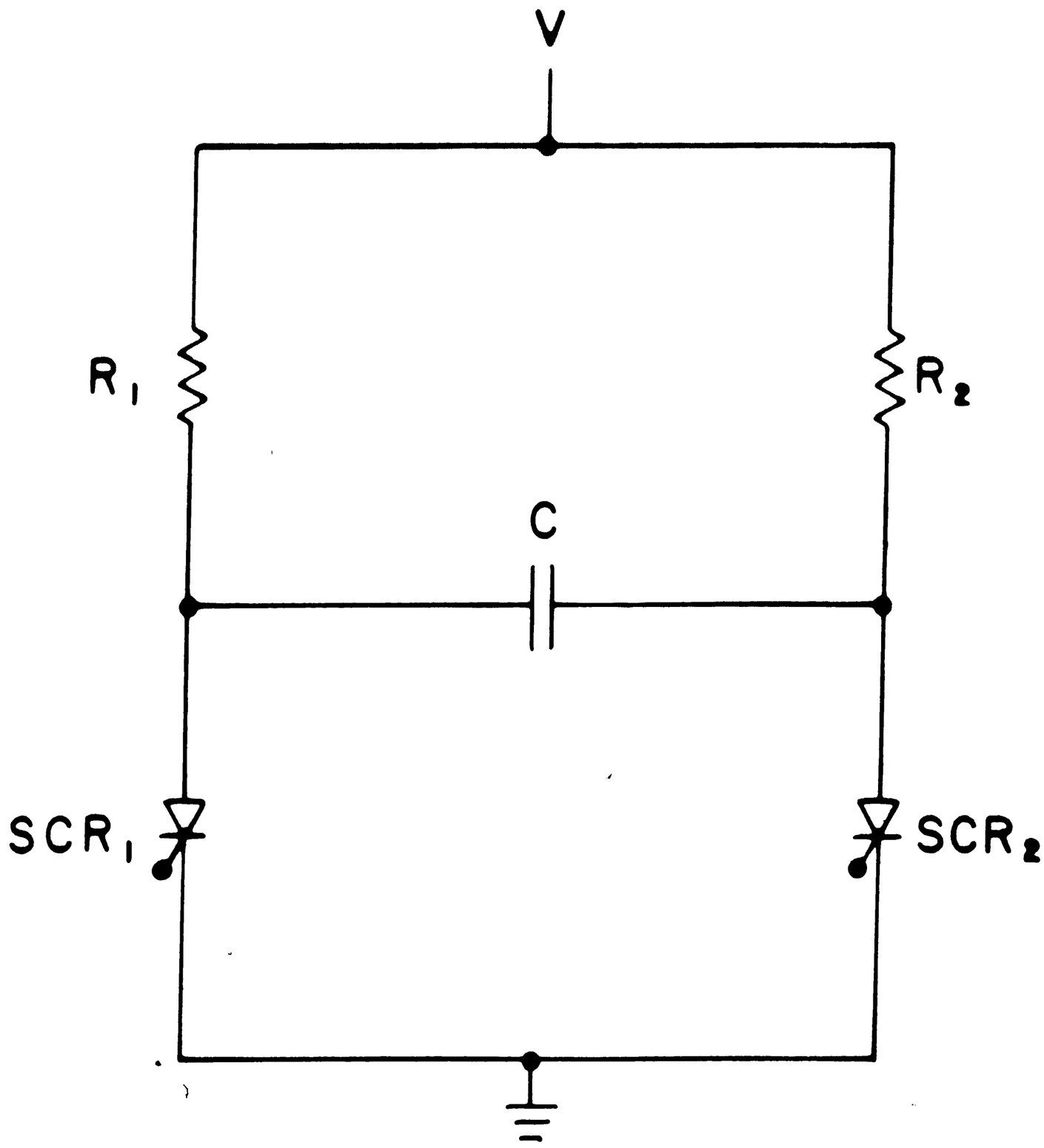
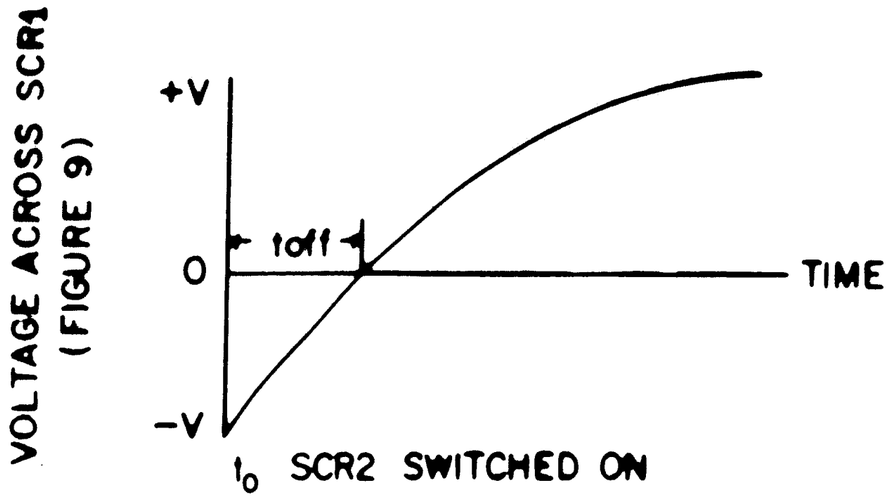
CASE NO.
39514-2

FIGURE 8



BASIC SCR DC SWITCH

FIGURE 9



NEGLECT VOLTAGE ACROSS SCR 2 (≈ 1V.)

$$V_{SCR1} = V_C = \frac{1}{C}\int_0^t i\,dt + \gamma$$

WHERE $\gamma = -V$

$$V_{SCR1} = 2V(1-e^{-t/R_1C}) - V$$

MINIMUM TIME CONSTANT (τ), $t = t_{off}$, $V_{SCR1} = 0$

$$V = 2V(1-e^{-t_{off}/R_1C})$$

$$e^{-t_{off}/R_1C} = .5$$

$$R_1C = 1.45\ t_{off}$$

$$\tau = R_1C = 1.45\ t_{off}$$

CALCULATION OF MINIMUM TIME CONSTANT

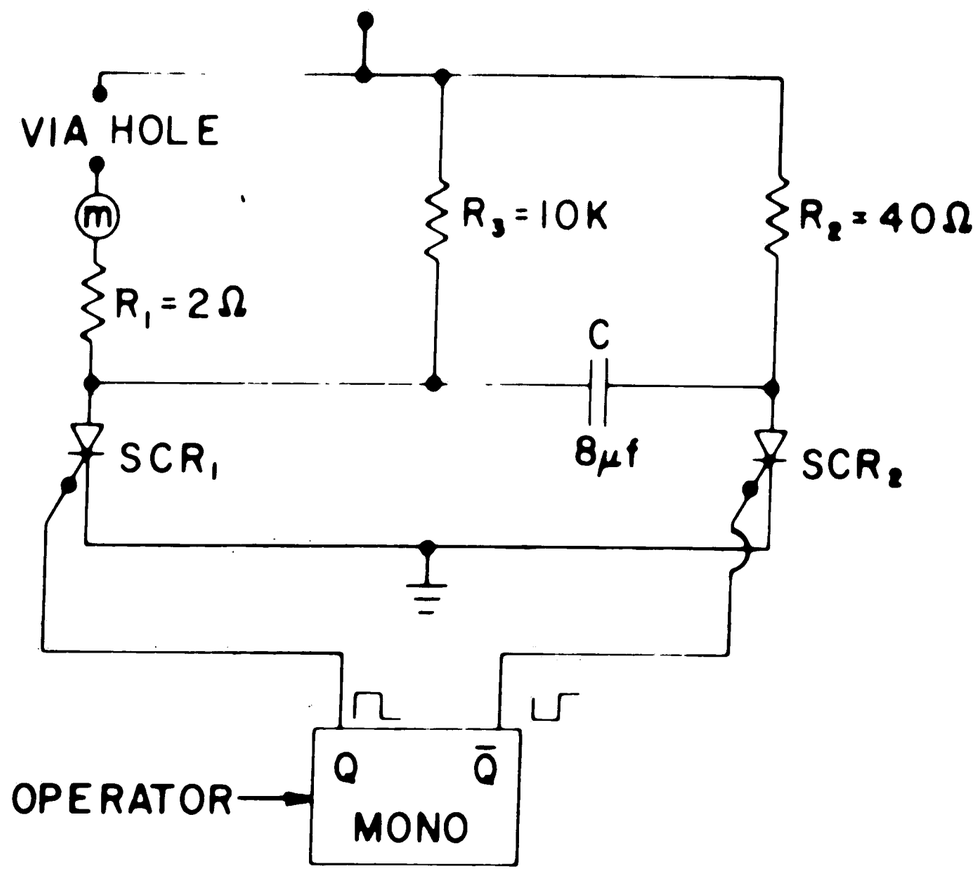
FIGURE 10

POWER SUPPLY - HARRISON LABORATORIES

MODEL 505A

0-72 VOLTS

0-5 AMPS



SCR_1 & SCR_2 - GE 11B (2N1774)

MIN. FORWARD BREAKOVER VOLTAGE	200 V
FORWARD CURRENT RMS	7.4 A
TURN OFF TIME toff	15μsec.

DETERMINATION R_1 Imax. @ 60 V = 20A, R_1eq = total resistance = 3Ω $\therefore$ $R_1 = 2\Omega$

$$C \geq \frac{1.5\,t_{off}}{R_1 eq} = 8\mu f$$

$$R_2 \leq \frac{\frac{1}{3}\,1\,msec.}{C} = 40\Omega$$

PROTOTYPE OVERLOAD TEST CIRCUIT

FIGURE 11

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B71-5841-AL

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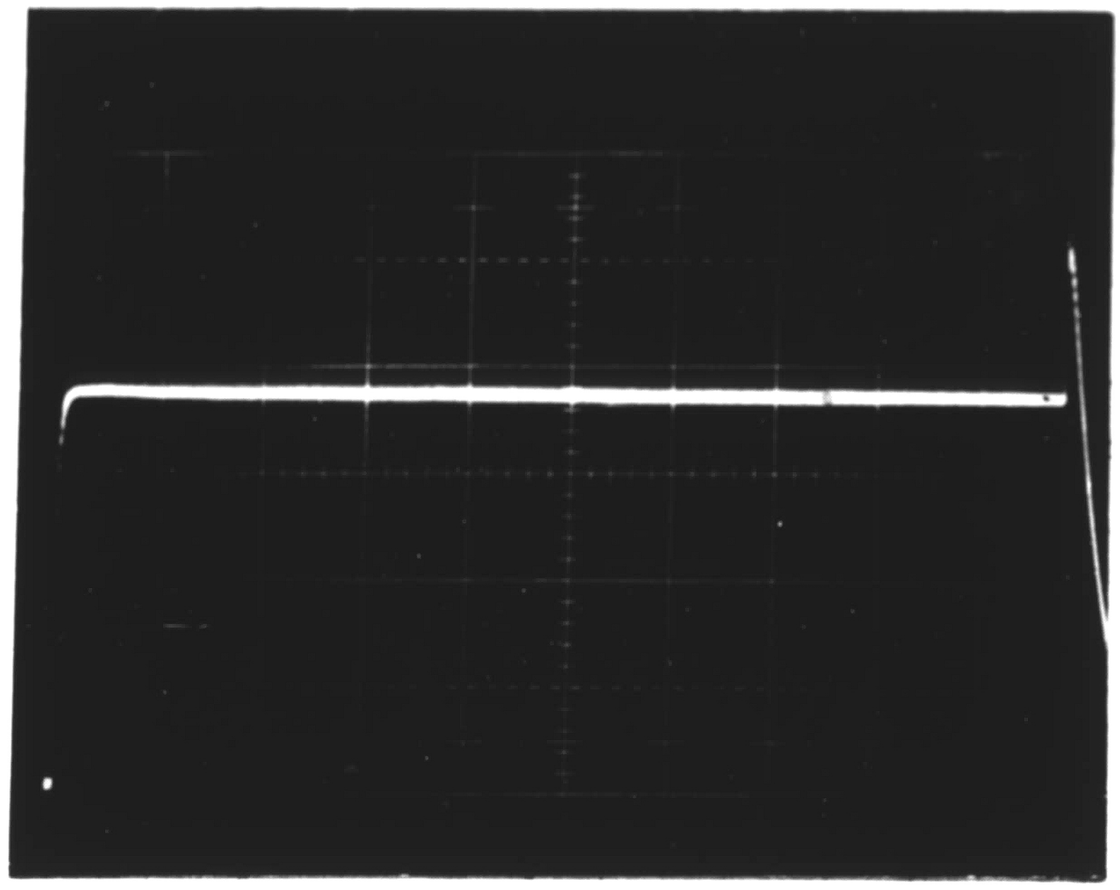
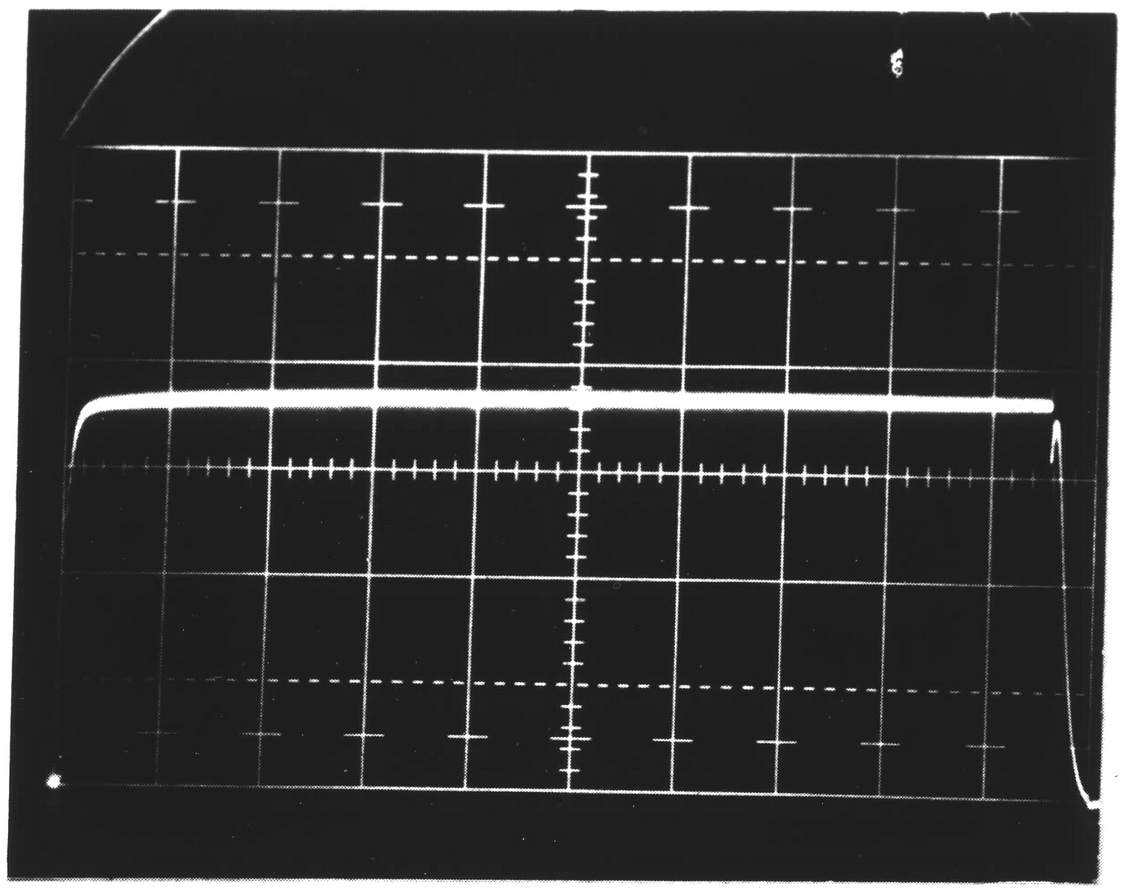
CASE NO.
39514-2



(a) BASIC SCR DC SWITCH

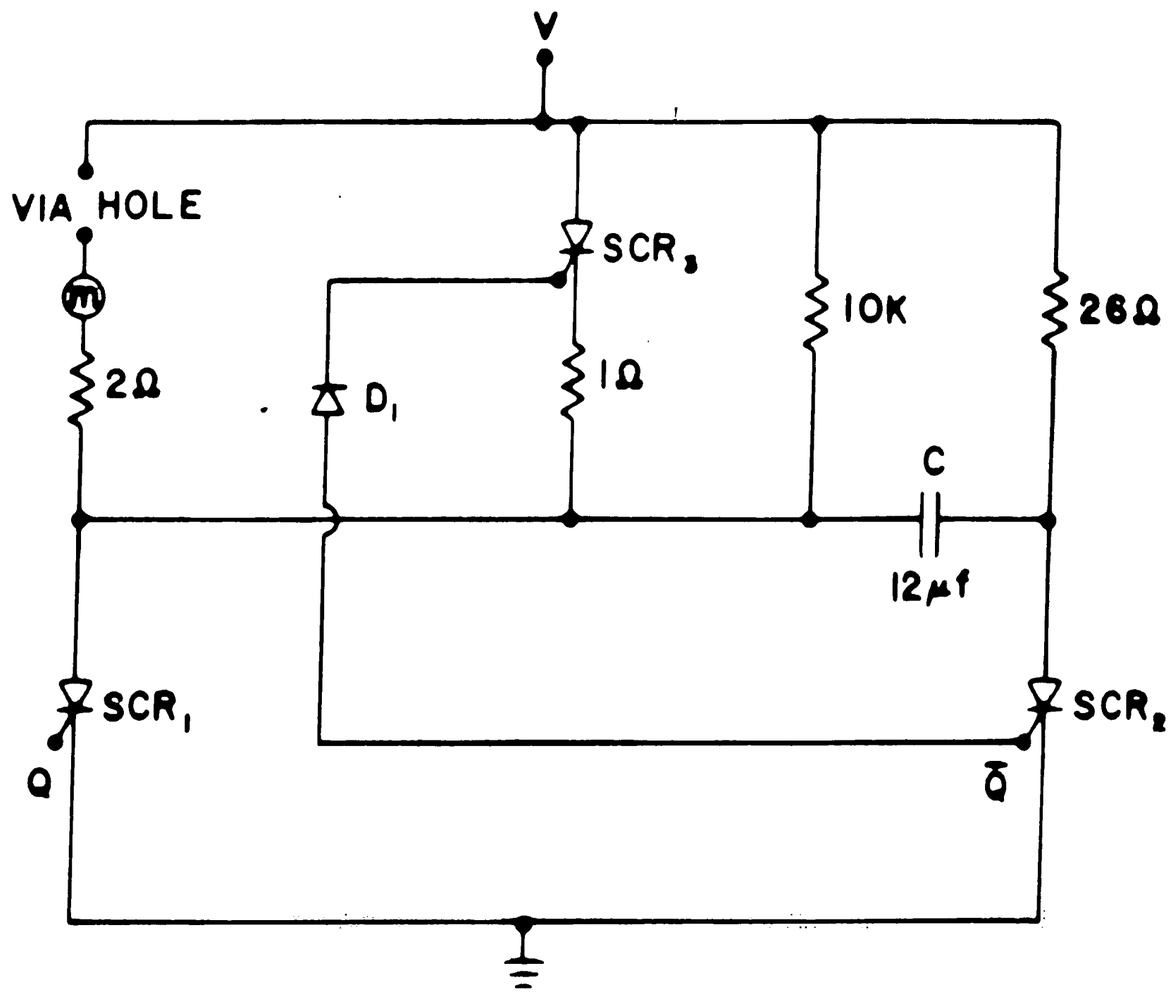
SCALE: VERT. 5A/cm, HOR. 0.1 msec./cm



(b) MODIFIED SCR DC SWITCH

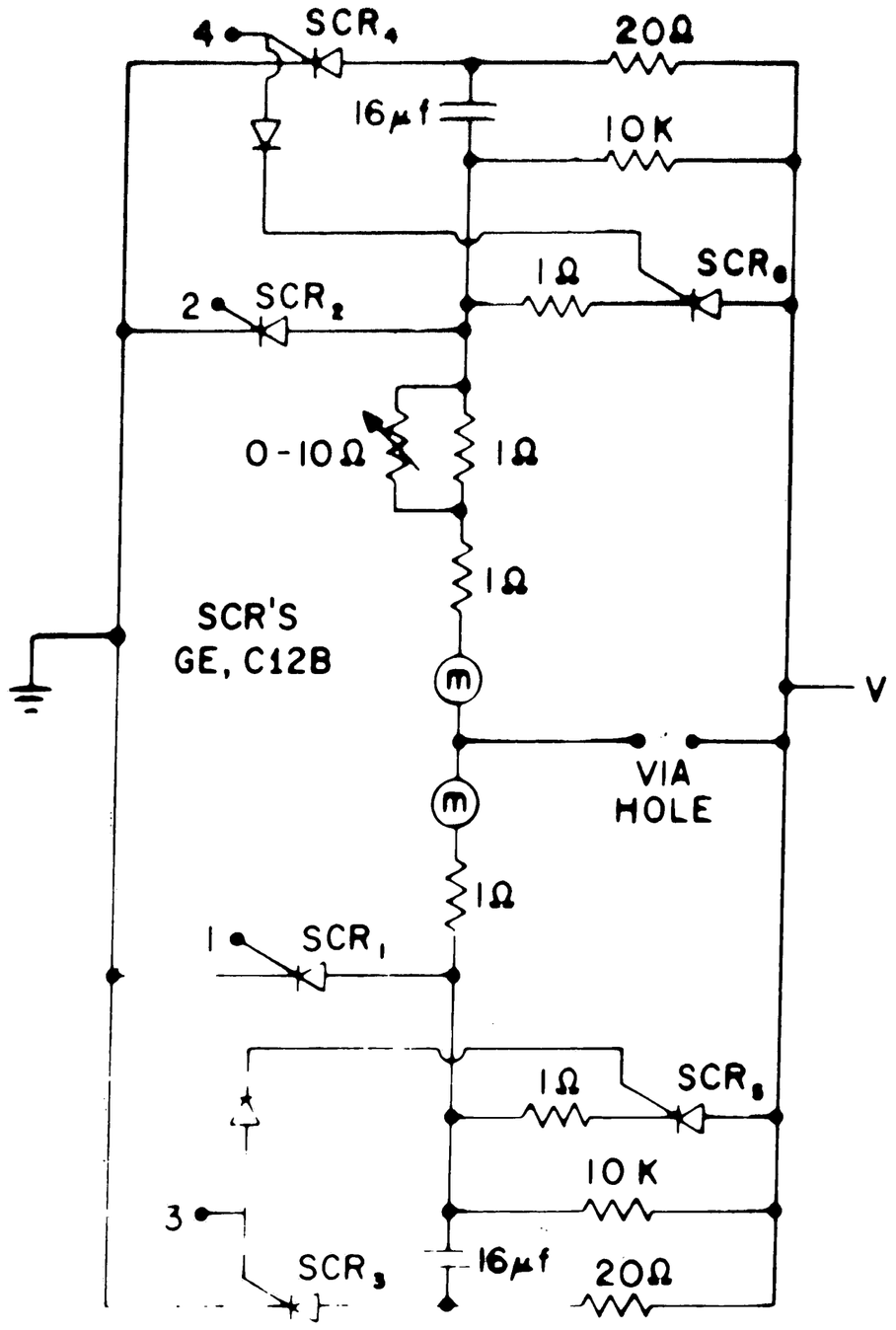
WAVEFORMS OF THE OVERLOAD TEST

FIGURE 12

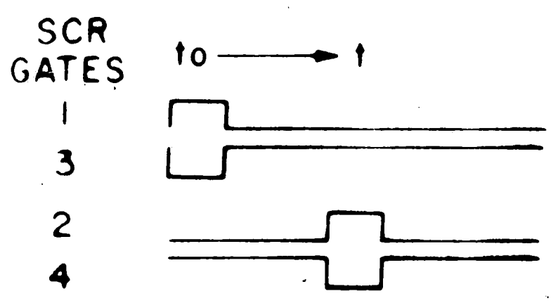


MODIFIED SCR DC SWITCH

FIGURE 13



TIMING TO GATES OF SCR'S



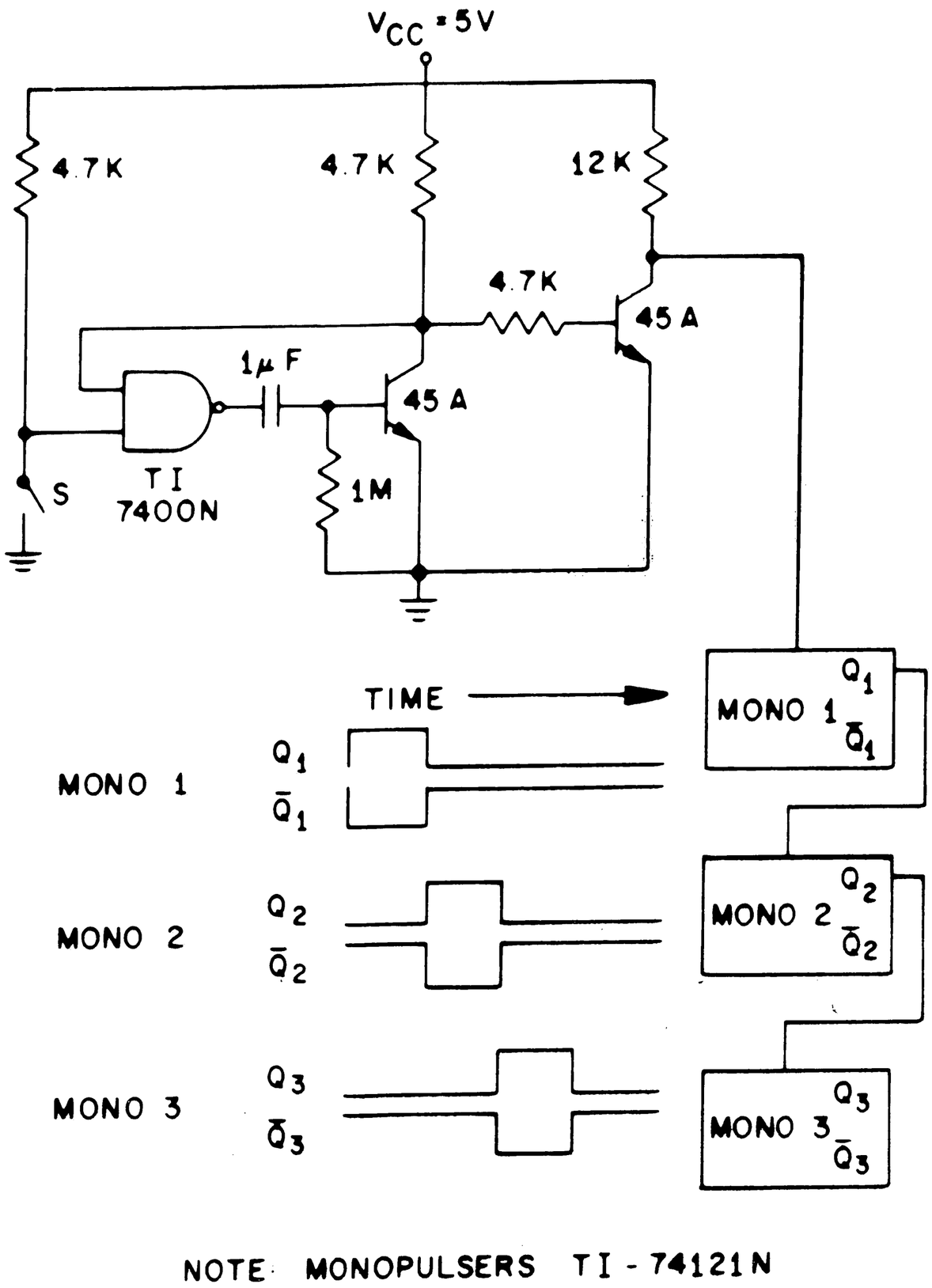
TWO PULSE-DIFFERENT AMPLITUDES-OVERLOAD TEST

FIGURE 14

BLOCK DIAGRAM

COMPLETE OVERLOAD TEST SET

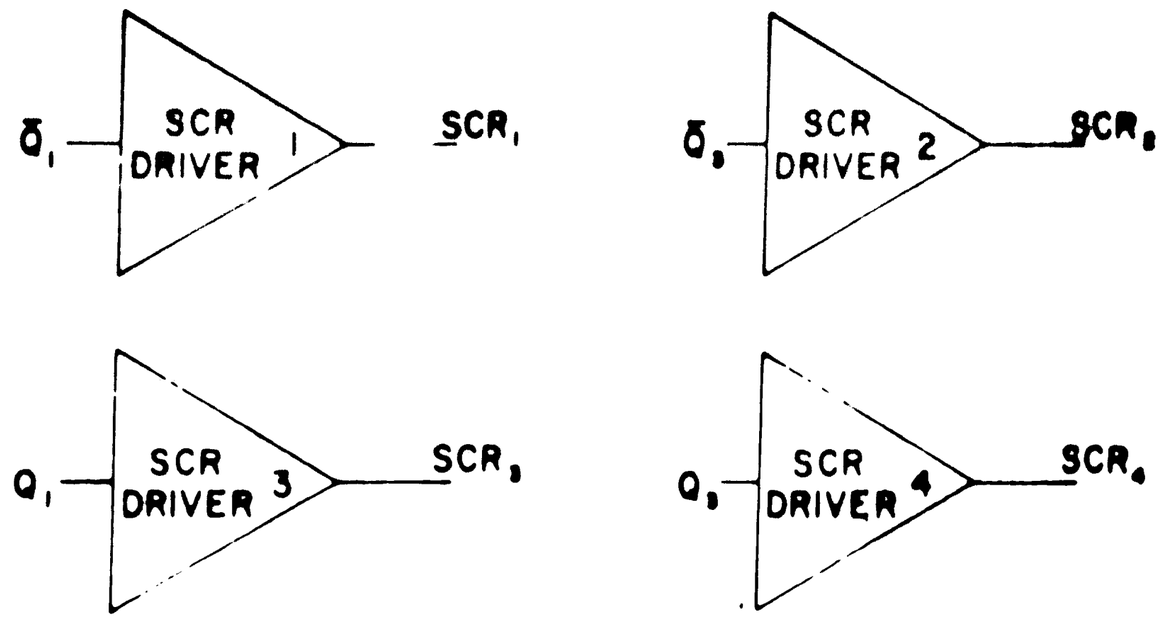
FIGURE 15



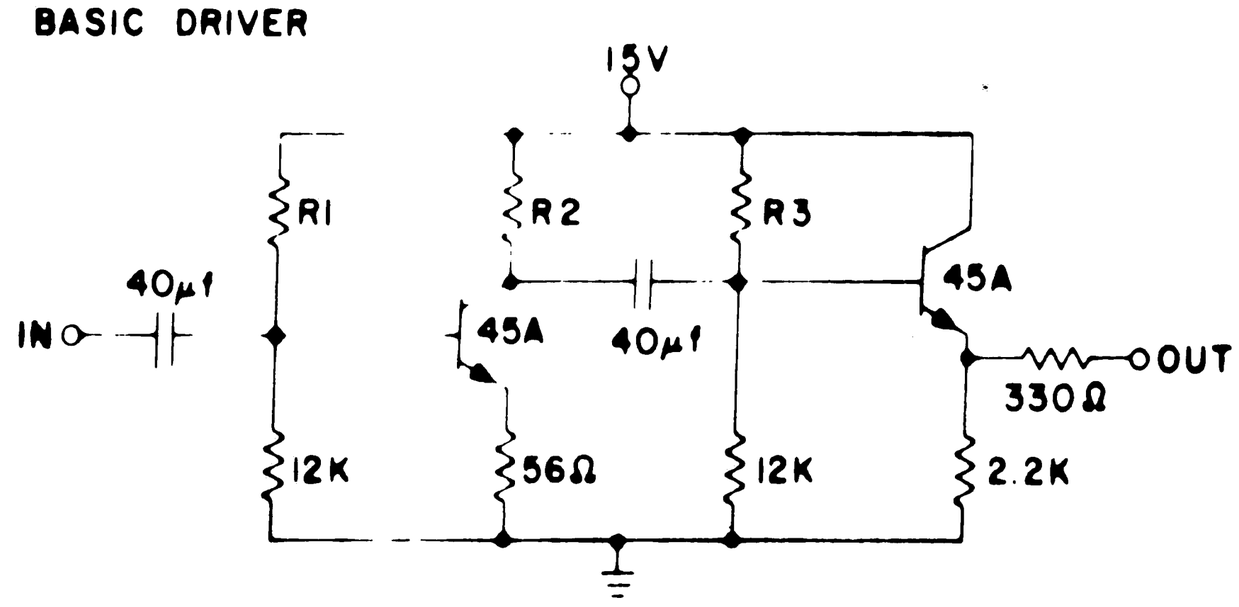
NOTE: MONOPULSERS TI - 74121N

CONTROL UNIT FOR OVERLOAD TEST SET

FIGURE 16



BASIC DRIVER



SCR DRIVERS	R_1	R_2	R_3
1 & 2	8.2K	560Ω	330K
3 & 4	330K	1K	2.2K

SCR DRIVERS

FIGURE 17

VITA

Mr. Robert N. Kershaw was born in Philadelphia, Pennsylvania, on January 3, 1941, the son of Mr. and Mrs. Nelson C. Kershaw. He graduated from Frankford High School, Philadelphia, Pennsylvania, in January 1959. He received a Certificate in Electronic Technology and an Associate Degree in Electronic Technology from Temple University in August 1960 and June 1963, respectively. He graduated Magna Cum Lauda with a Bachelor of Science Degree in Electrical Engineering from Lafayette College in June 1969. During the academic year 1969-1970 he attended the Pennsylvania State University Graduate Center at King of Prussia, Pennsylvania. He is a member of Eta Kappa Nu, Tau Beta Pi, and Phi Beta Kappa. From February 1961 to January 1963 he served in the U. S. Navy as an aviation electronic technician. From 1963 to 1969 he worked at the Bell Telephone Laboratories, Allentown, developing magnetic memory devices. He was a Product Engineer at Leeds and Northrup working in the Laboratory Equipment Division from 1969 to 1970. In 1970 he rejoined the Bell Telephone Laboratories and is presently an Associate Member of the Technical Staff. He is currently a member of the Material Development Department developing a technique for measuring the dielectric constant of alumina substrates. He and his wife, the former Joy M. King, and their four children, Lisa, Bobby, Scott and Dale reside in Harleysville, Pennsylvania.